

NCP51145

DDR 1.8 Amp Source / Sink V_{TT} Termination Regulator

The NCP51145 is a linear regulator designed to supply a regulated V_{TT} termination voltage for DDR-II, DDR-III, LPDDR-III and DDR-IV memory applications. The regulator is capable of actively sourcing and sinking ±1.8 A peak currents while regulating an output voltage to within ±20 mV. The output termination voltage is regulated to track V_{DDQ} / 2 by two external voltage divider resistors connected to the PV_{CC}, GND, and V_{REF} pins.

The NCP51145 incorporates a high-speed differential amplifier to provide ultra-fast response to line and load transients. Other features include source/sink current limiting, soft-start and on-chip thermal shutdown protection.

Features

- For DDR V_{TT} Applications, Source/Sink Currents:
- Supports DDR-II to ±1.8 A, DDR-III to ±1.5 A
- Supports LPDDR-III and DDR-IV to ±1.2 A
- Stable Using Ceramic-Only (Very Low ESR) Capacitors
- Integrated Power MOSFETs
- High Accuracy V_{TT} Output at Full-Load
- Fast Transient Response
- Built-in Soft-Start
- Shutdown for Standby or Suspend Mode
- Integrated Thermal and Current-Limit Protection
- V_{TT} Remote Sense Available in the DFN8 2x2mm Package
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

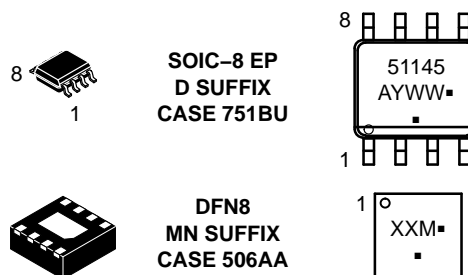
- DDR-II / DR-III / DDR-IV SDRAM Termination Voltage
- Motherboard, Notebook, and VGA Card Memory Termination
- Set Top Box, Digital TV, Printers
- Low Power DDR-3LP



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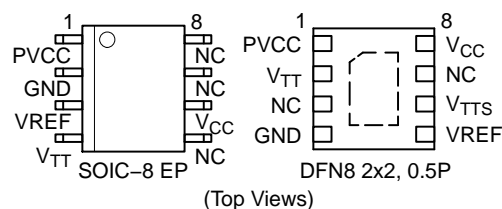
MARKING DIAGRAMS



51145 = Specific Device Code
 XX = Specific Device Code
 M = Date Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping [†]
NCP51145PDR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCP51145MNTAG	DFN-8 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP51145

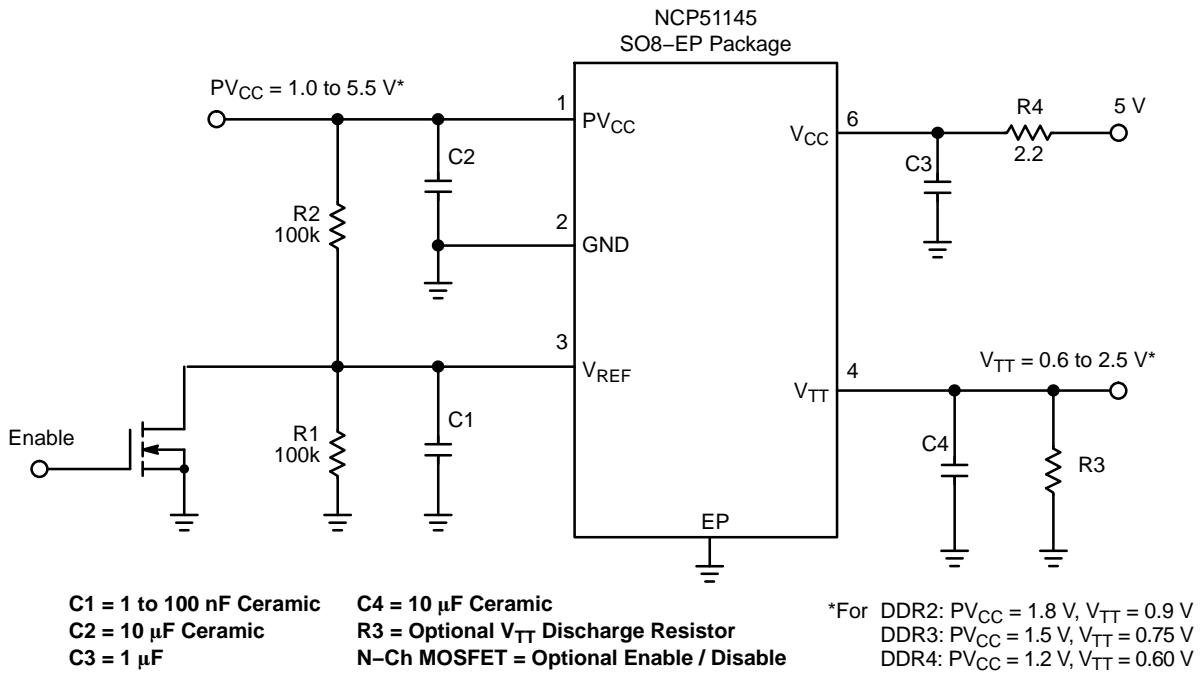


Figure 1. Application Diagram

PIN FUNCTION DESCRIPTION

Pin No. SO8-EP	Pin No. DFN8	Pin Name	Description
1	1	PV _{CC}	Input voltage which supplies current to the output pin. $C_{IN} \cong \frac{1}{2} \cdot C_{OUT}$
2	4	GND	Common Ground
3	5	V _{REF}	Buffered reference voltage input equal to $\frac{1}{2}$ of V _{DDQ} and active low shutdown pin. An external resistor divider dividing down the PV _{CC} voltage creates the regulated output voltage. Pulling the pin to ground (0.15 V maximum) turns the device off.
4	2	V _{TT}	Regulator output voltage capable of sourcing and sinking current while regulating the output rail. C _{OUT} = 10 μF Ceramic, or greater
5, 7, 8	3, 7	NC	True No Connect
6	8	V _{CC}	The V _{CC} pin is a 5 V input pin that provides internal bias to the controller. PV _{CC} should always be kept lower or equal to V _{CC} .
-	6	V _{TTS}	V _{TT} Sense
EP	EP	EPAD	Pad for thermal connection. The exposed pad must be connected to the ground plane using multiple vias for maximum power dissipation performance.

NCP51145

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Supply Voltage Range ($V_{CC} \geq PV_{CC}$) (Note 1)	PV_{CC}, V_{CC}	-0.3 to 6	V
Output Voltage Range	V_{TT}	-0.3 to 6	V
Reference Input Range	V_{REF}	-0.3 to 6	V
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	TSTG	-65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESDHBM	2	kV
ESD Capability, Machine Model (Note 2)	ESDMM	200	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)
Latchup Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SO8-EP (Note 4) Thermal Resistance, Junction-to-Air (Note 5) Thermal Reference, Junction-to-Lead2 (Note 5)	$R_{\theta JA}$ $R_{\psi JL}$	82 TBD	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm² (or 1 in²) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 6)

Rating	Symbol	Min	Max	Unit
Input Voltage	PV_{CC}	1.0	5.5	V
Bias Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	-40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

NCP51145

ELECTRICAL CHARACTERISTICS

$PV_{CC} = 1.8\text{ V} / 1.5\text{ V}$; $V_{CC} = 5\text{ V}$; $V_{REF} = 0.9\text{ V} / 0.75\text{ V}$; $C_{TT} = 10\text{ }\mu\text{F}$ (Ceramic), $T_A = +25^\circ\text{C}$, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
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REGULATOR OUTPUT

Output Offset Voltage	$I_{out} = 0\text{ A}$	V_{OS}	-16	-	+16	mV
Load Regulation	$I_{out} = \pm 1.8\text{ A}$, $PV_{CC} = 1.8\text{ V}$, $V_{REF} = 0.9\text{ V}$	Reg_{load}	-4	-	+4	mV
	$I_{out} = \pm 1.5\text{ A}$, $PV_{CC} = 1.5\text{ V}$, $V_{REF} = 0.75\text{ V}$					
	$I_{out} = \pm 1.2\text{ A}$, $PV_{CC} = 1.35\text{ V}$, $V_{REF} = 0.675\text{ V}$					
	$I_{out} = \pm 1.2\text{ A}$, $PV_{CC} = 1.2\text{ V}$, $V_{REF} = 0.6\text{ V}$					

INPUT AND STANDBY CURRENTS

Bias Supply Current	$I_{out} = 0\text{ A}$	I_{BIAS}	-	1	2.5	mA
Standby Current	$V_{REF} < 0.2\text{ V}$ (Shutdown), $R_{LOAD} = 180\Omega$	I_{STB}	-	2	90	μA

CURRENT LIMIT PROTECTION

Current Limit	$PV_{CC} = 1.8\text{ V}$, $V_{REF} = 0.9\text{ V}$	I_{LIM}	2	-	3.5	A
	$PV_{CC} = 1.5\text{ V}$, $V_{REF} = 0.75\text{ V}$		1.5	-	3.5	

SHUTDOWN THRESHOLDS

Shutdown Threshold Voltage	Enable	V_{IH}	0.45	-	-	V
	Shutdown	V_{IL}	-	-	0.15	

THERMAL SHUTDOWN

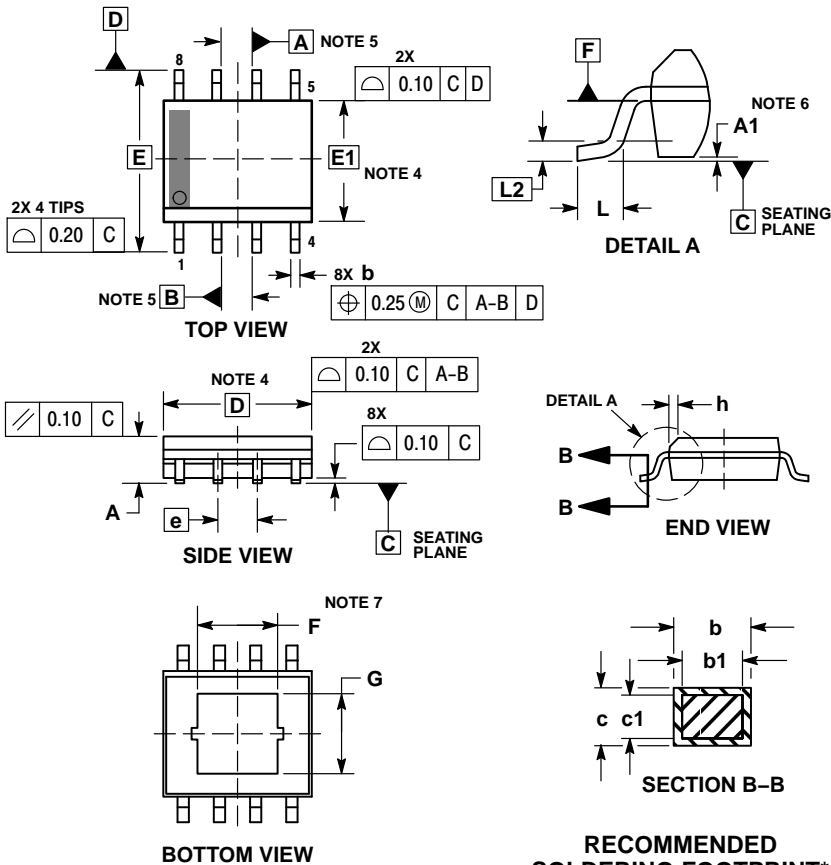
Thermal Shutdown Temperature	$V_{CC} = 5\text{ V}$	T_{SD}	-	125	-	$^\circ\text{C}$
Thermal Shutdown Hysteresis	$V_{CC} = 5\text{ V}$	T_{SH}	-	35	-	$^\circ\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NCP51145

PACKAGE DIMENSIONS

SOIC8-NB EP CASE 751BU ISSUE E

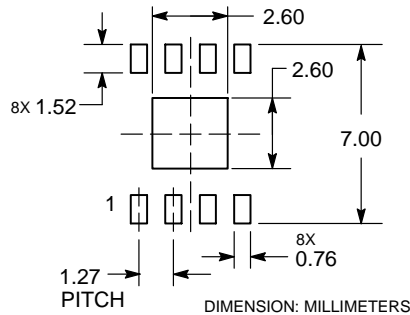


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. TAB CONTOUR MAY VARY MINIMALLY TO INCLUDE TOOLING FEATURES.

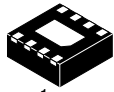
DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
F	1.55	2.39
G	1.55	2.39
h	0.25	0.50
L	0.40	1.27
L2	0.25 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

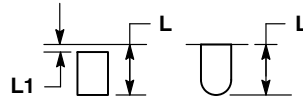
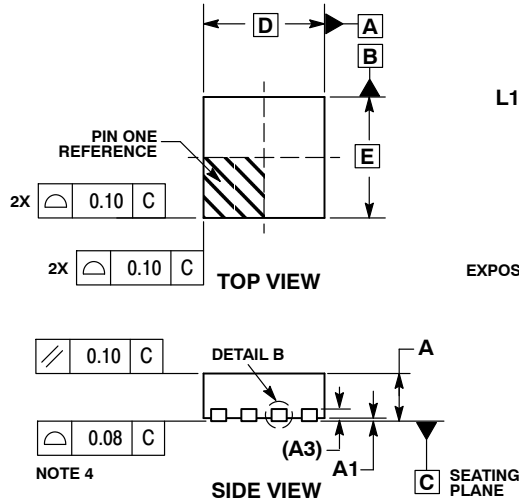
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



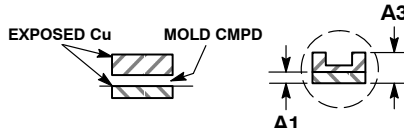
SCALE 4:1

DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

DATE 04 MAY 2016



DETAIL A
OPTIONAL
CONSTRUCTIONS



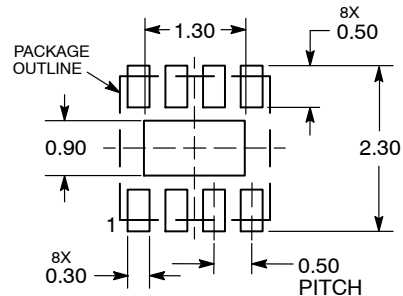
DETAIL B
ALTERNATE
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

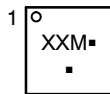
DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.10	1.30
E	2.00	BSC
E2	0.70	0.90
e	0.50	BSC
K	0.30	REF
L	0.25	0.35
L1	---	0.10

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN8, 2.0X2.0, 0.5MM PITCH	PAGE 1 OF 1

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