

# NCP2993

## Audio Power Amplifier, 1.3 W, with Selectable Fast Turn-On Time

The NCP2993 is an audio power amplifier designed for portable communication device applications such as mobile phone applications. The NCP2993 is capable of delivering 1.3 W of continuous average power to an 8.0  $\Omega$  BTL load from a 5.0 V power supply, and 1.1 W to a 4.0  $\Omega$  BTL load from a 3.6 V power supply.

The NCP2993 provides high quality audio while requiring few external components and minimal power consumption. It features a low-power consumption shutdown mode, which is achieved by driving the SHUTDOWN pin with logic low.

The NCP2993 contains circuitry to prevent from “pop and click” noise that would otherwise occur during turn-on and turn-off transitions. It is a zero pop noise device when a single ended or a differential audio input is used.

For maximum flexibility, the NCP2993 provides an externally controlled gain (with resistors). In addition, it integrates 2 different Turn On times (15 ms or 30 ms) adjustable with the TON pin.

Due to its superior PSRR, it can be directly connected to the battery, saving the use of an LDO.

This device is available in a 9-Pin Flip-Chip CSP package with a 0.4mm pitch (Lead-Free).

### Features

- 1.3 W to an 8.0  $\Omega$  BTL Load from a 5.0 V Power Supply
- Best-in-Class PSRR: up to -88 dB, Direct Connection to the Battery
- Zero Pop Noise Signature with a Single Ended Audio Input
- Ultra Low Current Shutdown Mode: 10 nA
- 2.5 V–5.5 V Operation
- External Gain Configuration Capability
- External Turn-on Time Configuration Capability: 15 ms or 30 ms
- Thermal Overload Protection Circuitry
- This is a Pb-Free Device\*

### Typical Applications

- Portable Electronic Devices
- PDAs
- Wireless Phones



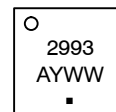
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM

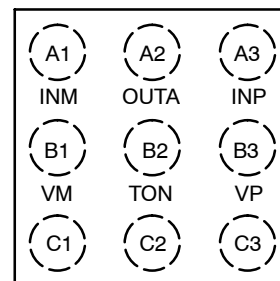


WLCSP9  
FC SUFFIX  
CASE 499BM



2993 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

### PIN CONNECTIONS



BYPASS OUTB SHUTDOWN  
(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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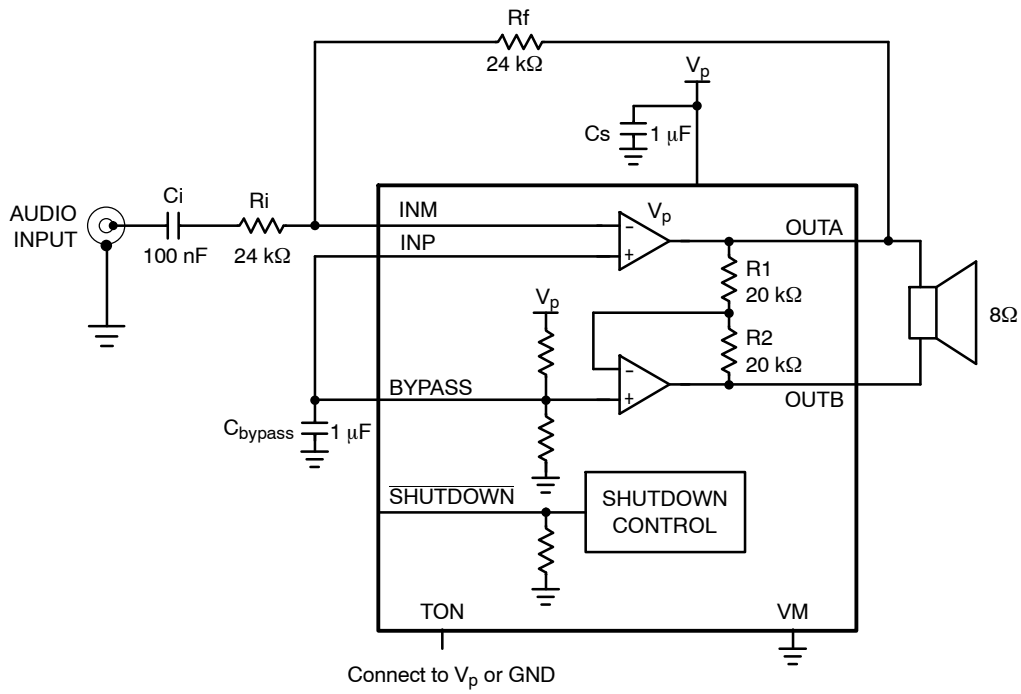


Figure 1. Typical Audio Amplifier Application Circuit with Single Ended Input

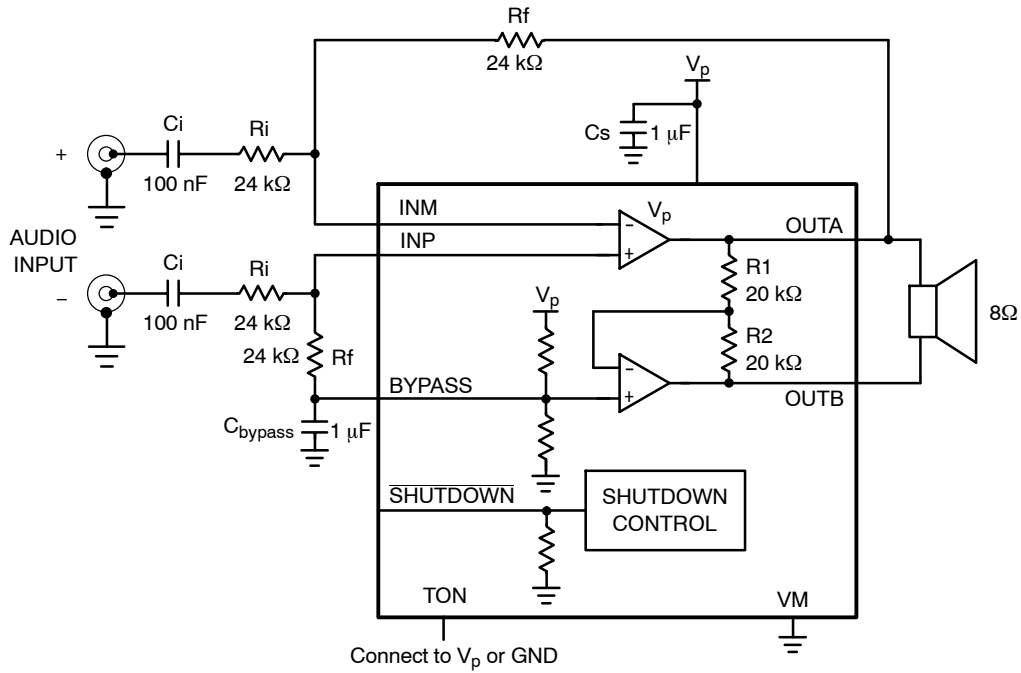


Figure 2. Typical Audio Amplifier Application Circuit with a Differential Input

# NCP2993

## PIN DESCRIPTION

Pin	Name	Type	Description
A1	INM	I	Negative input of the first amplifier, receives the audio input signal. Connected to the feedback resistor $R_f$ and to the input resistor $R_{in}$ .
A2	OUTA	O	Negative output of the NCP2993. Connected to the load and to the feedback resistor $R_f$ .
A3	INP	I	Positive input of the first amplifier, receives the common mode voltage.
B1	VM	I	Analog Ground.
B2	TON	I	TON pin selects 2 different Turn On times: TON = GND $\rightarrow$ 30 ms TON = VP $\rightarrow$ 15 ms
B3	VP	I	Positive analog supply of the cell. Range: 2.5 V–5.5 V.
C1	BYPASS	I	Bypass capacitor pin which provides the common mode voltage ( $V_p/2$ ).
C2	OUTB	O	Positive output of the NCP2993. Connected to the load.
C3	SHUTDOWN	I	The device enters in shutdown mode when a low level is applied on this pin.

## MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	$V_p$	6.0	V
Operating Supply Voltage	Op $V_p$	2.5 to 5.5 V	–
Input Voltage	$V_{in}$	–0.3 to $V_{CC} + 0.3$	V
Power Dissipation (Note 2)	$P_d$	Internally Limited	–
Operating Ambient Temperature	$T_A$	–40 to +85	°C
Max Junction Temperature	$T_J$	150	°C
Storage Temperature Range	$T_{stg}$	–65 to +150	°C
Thermal Resistance Junction–to–Air	$R_{\theta JA}$	(Note 3)	°C/W
ESD Protection	Human Body Model (HBM) (Note 4)	2000	V
	Machine Model (MM) (Note 5)	200	
Latchup Current @ $T_A = 85^\circ\text{C}$ (Note 6)	–	$\pm 100$	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at  $T_A = +25^\circ\text{C}$ .
2. The thermal shutdown set to  $160^\circ\text{C}$  (typical) avoids irreversible damage on the device due to power dissipation.
3. The  $R_{\theta JA}$  is highly dependent of the PCB Heatsink area. For example,  $R_{\theta JA}$  can equal  $195^\circ\text{C/W}$  with  $50\text{ mm}^2$  total area and also  $135^\circ\text{C/W}$  with  $500\text{ mm}^2$ . The bumps have the same thermal resistance and all need to be connected to optimize the power dissipation.
4. Human Body Model, 100 pF discharge through a  $1.5\text{ k}\Omega$  resistor following specification JESD22/A114.
5. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

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**ELECTRICAL CHARACTERISTICS** Limits apply for  $T_A$  between  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (Unless otherwise noted).

Characteristic	Symbol	Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit	
Supply Quiescent Current	$I_{dd}$	$V_p = 2.5\text{ V}$ , No Load	-	1.8	3.5	mA	
		$V_p = 5.0\text{ V}$ , No Load	-	1.95			
		$V_p = 2.5\text{ V}$ , $8\ \Omega$ $V_p = 5.0\text{ V}$ , $8\ \Omega$	-	1.8 1.95	3.5		
Common Mode Voltage	$V_{cm}$	-	-	$V_p/2$	-	V	
Shutdown Current	$I_{SD}$	-	-	0.02	0.5	$\mu\text{A}$	
Shutdown Pull-Down	$R_{SD}$	-	-	300	-	k $\Omega$	
Shutdown Voltage High	$V_{SDIH}$	-	1.2	-	-	V	
Shutdown Voltage Low	$V_{SDIL}$	-	-	-	0.4	V	
Turn On Time (Note 8)	$T_{WU}$	TON = GND	-	30	-	ms	
		TON = VP	-	15			
Turn Off Time	$T_{OFF}$	-	-	1.0	-	$\mu\text{s}$	
Output Impedance in Shutdown Mode	$Z_{SD}$	-	-	8.5	-	k $\Omega$	
Output Swing	$V_{loadpeak}$	$V_p = 2.5\text{ V}$ , $R_L = 8.0\ \Omega$	1.9	2.3	-	V	
		$V_p = 5.0\text{ V}$ , $R_L = 8.0\ \Omega$ (Note 7) $T_A = +25^{\circ}\text{C}$	3.8	4.6	-		
RMS Output Power	$P_O$	$V_p = 2.5\text{ V}$ , $R_L = 4.0\ \Omega$ THD + N < 1%	-	0.5	-	W	
		$V_p = 2.5\text{ V}$ , $R_L = 8.0\ \Omega$ THD + N < 1%	-	0.32	-		
		$V_p = 5.0\text{ V}$ , $R_L = 8.0\ \Omega$ THD + N < 1%	-	1.3	-		
Maximum Power Dissipation (Note 8)	$P_{Dmax}$	$V_p = 5.0\text{ V}$ , $R_L = 8.0\ \Omega$	-	-	0.65	W	
Output Offset Voltage	$V_{OS}$	$V_p = 2.5\text{ V}$ $V_p = 5.0\text{ V}$	-	1.0	-	mV	
Signal-to-Noise Ratio	SNR	$V_p = 2.5\text{ V}$ , $G = 2.0$ 20 Hz < F < 20 kHz	-	91	-	dB	
Positive Supply Rejection Ratio	PSRR V+	$G = 2.0$ , $R_L = 8.0\ \Omega$ $C_{by} = 1.0\ \mu\text{F}$ Input Grounded F = 217 Hz	-	-88	-	dB	
			$V_p = 5.0\text{ V}$	-	-88		-
			$V_p = 4.2\text{ V}$	-	-88		-
		$V_p = 3.0\text{ V}$	-	-88	-		
		F = 1.0 kHz	-	-88	-		
			$V_p = 5.0\text{ V}$	-	-88		-
$V_p = 4.2\text{ V}$	-		-88	-			
Efficiency	$\eta$	$V_p = 2.5\text{ V}$ , $P_{orms} = 320\text{ mW}$	-	70	-	%	
		$V_p = 5.0\text{ V}$ , $P_{orms} = 1.0\text{ W}$	-	60	-		
Thermal Shutdown Temperature	$T_{sd}$	-	-	160	-	$^{\circ}\text{C}$	
Total Harmonic Distortion	THD	$V_p = 2.5\text{ V}$ , F = 1.0 kHz $R_L = 4.0\ \Omega$ , $A_V = 2.0$ $P_O = 0.32\text{ W}$	-	-	-	%	
			-	0.015	-		
		$V_p = 5.0\text{ V}$ , F = 1.0 kHz $R_L = 8.0\ \Omega$ , $A_V = 2.0$ $P_O = 1.0\text{ W}$	-	-	-		
			-	0.01	-		

6. Min/Max limits are guaranteed by design, test or statistical analysis.

7. This parameter is guaranteed but not tested in production in case of a 5.0 V power supply.

8. See page 10 for a theoretical approach of this parameter.

TYPICAL CHARACTERISTICS

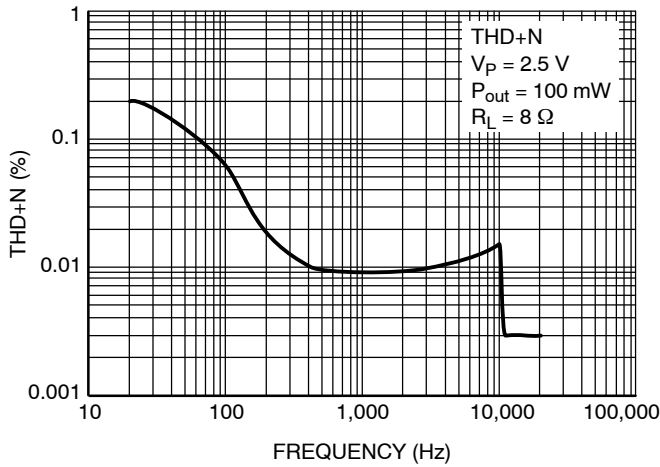


Figure 3. THD+N vs. Frequency, Single-Ended Input

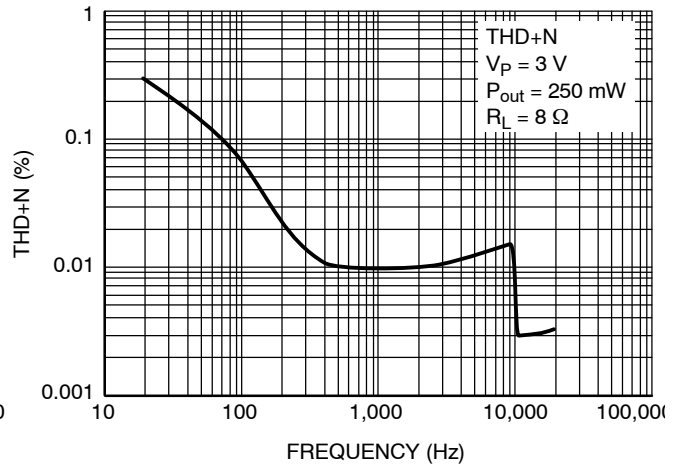


Figure 4. THD+N vs. Frequency, Single-Ended Input

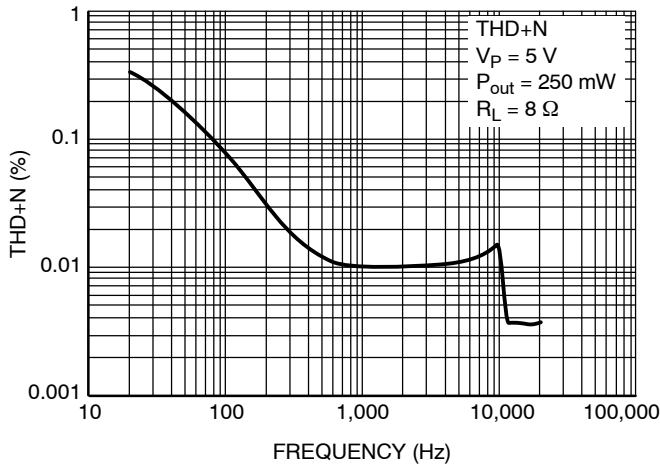


Figure 5. THD+N vs. Frequency, Single-Ended Input

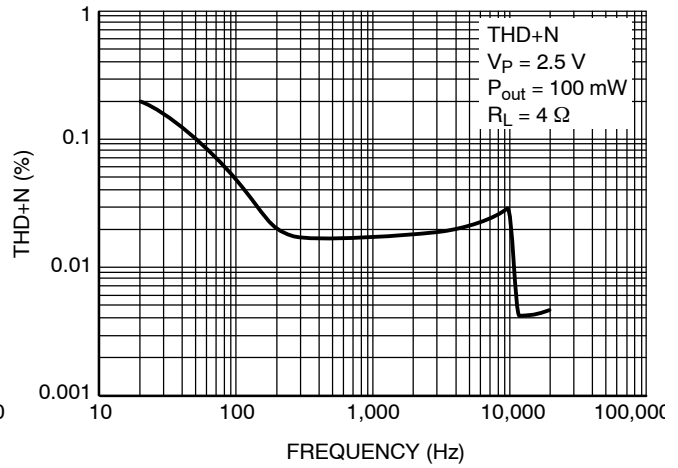


Figure 6. THD+N vs. Frequency, Single-Ended Input

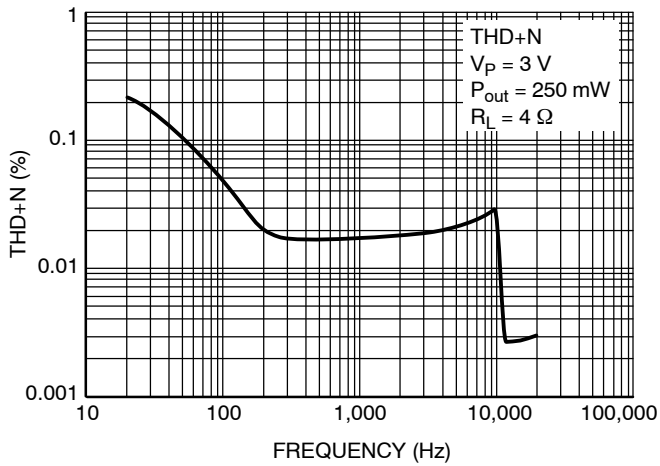


Figure 7. THD+N vs. Frequency, Single-Ended Input

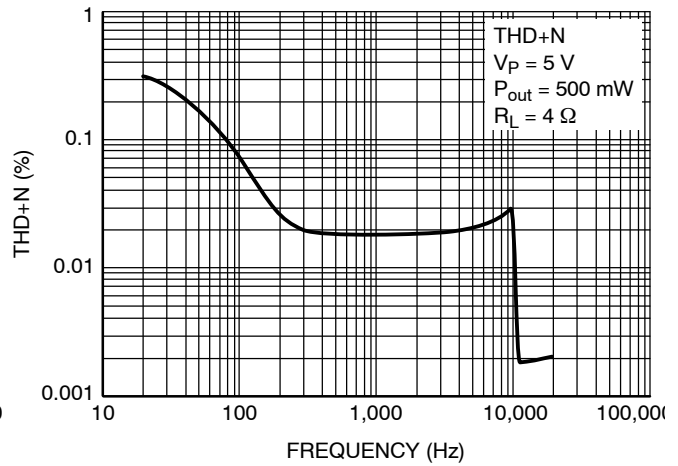


Figure 8. THD+N vs. Frequency, Single-Ended Input

TYPICAL CHARACTERISTICS

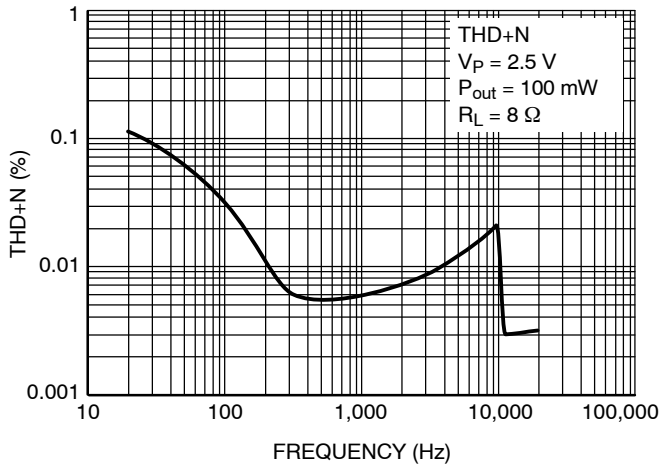


Figure 9. THD+N vs. Frequency, Differential Input

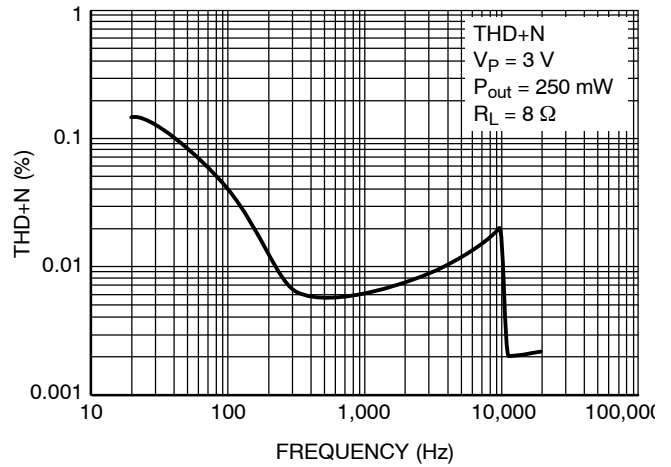


Figure 10. THD+N vs. Frequency, Differential Input

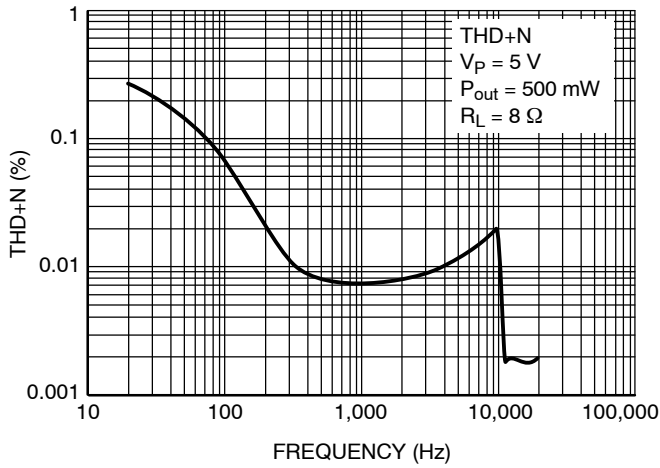


Figure 11. THD+N vs. Frequency, Differential Input

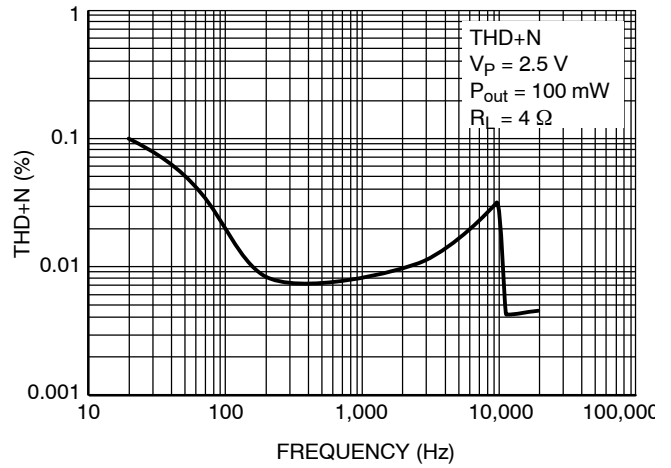


Figure 12. THD+N vs. Frequency, Differential Input

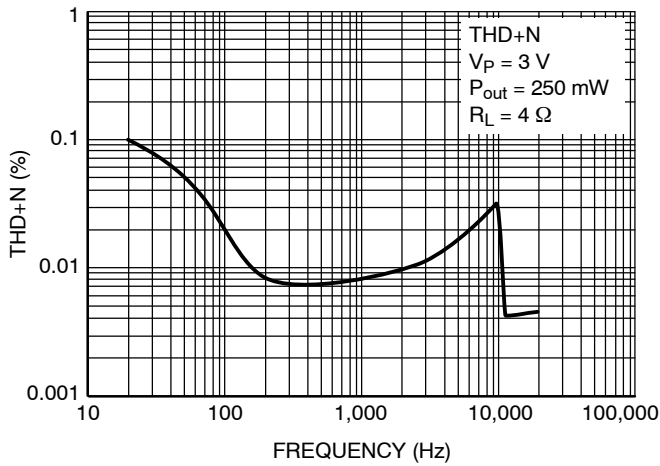


Figure 13. THD+N vs. Frequency, Differential Input

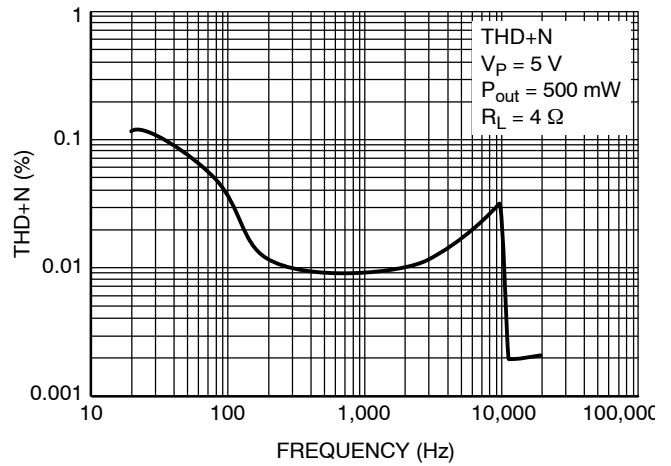


Figure 14. THD+N vs. Frequency, Differential Input

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## TYPICAL CHARACTERISTICS

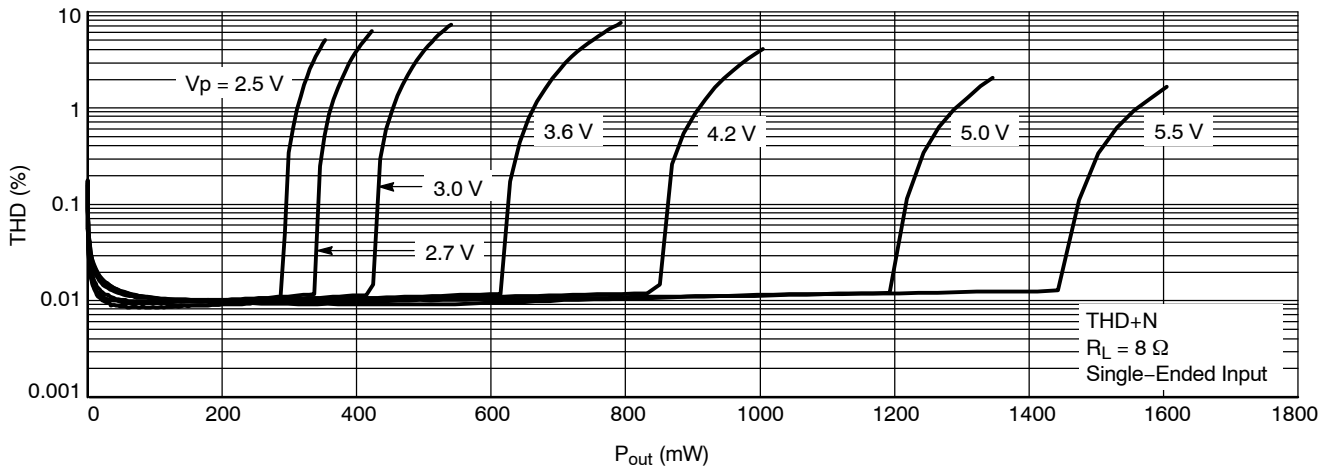


Figure 15. THD+N vs.  $P_{out}$

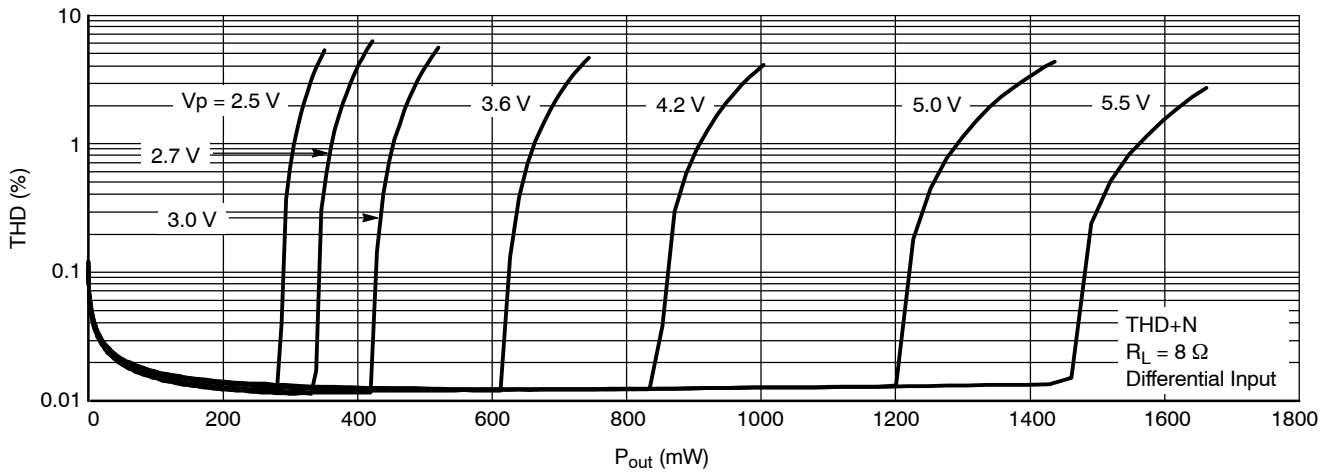


Figure 16. THD+N vs.  $P_{out}$

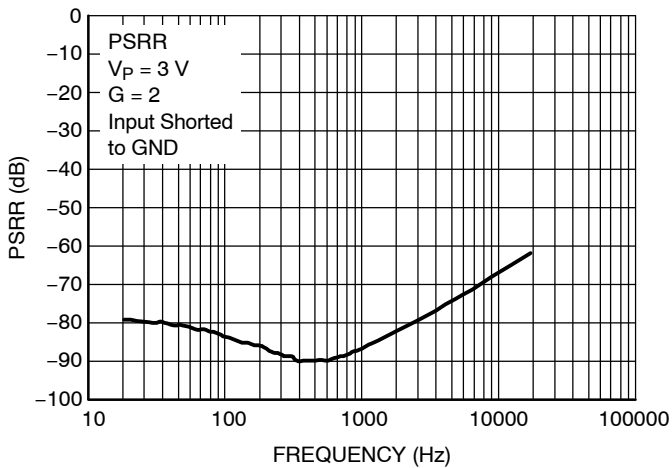


Figure 17. PSRR vs. Frequency

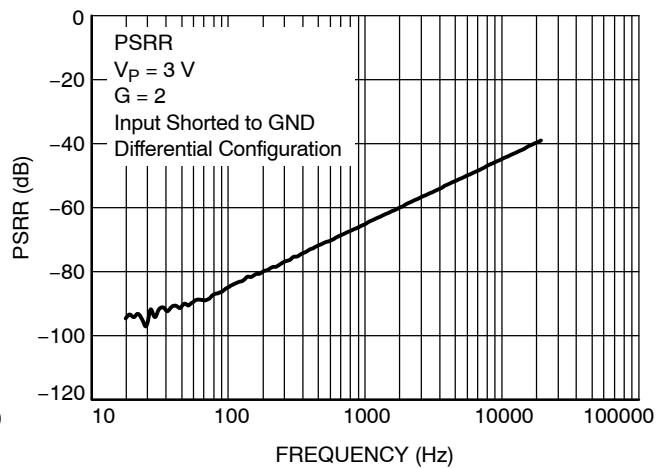


Figure 18. PSRR vs. Frequency

TYPICAL CHARACTERISTICS

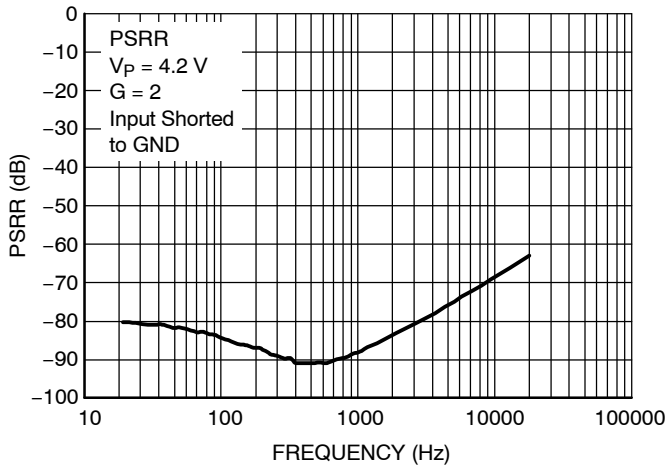


Figure 19. PSRR vs. Frequency

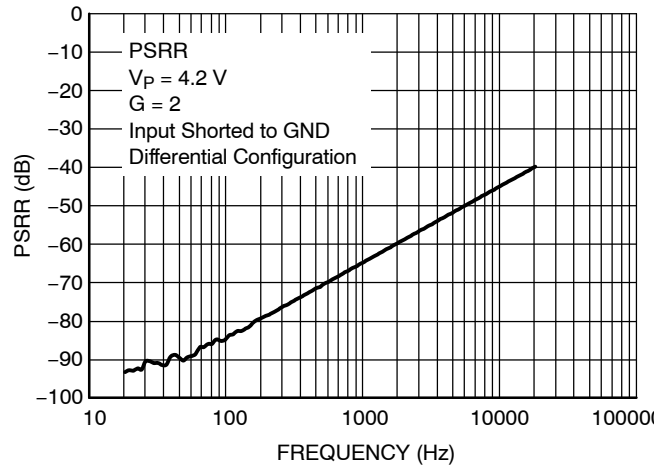


Figure 20. PSRR vs. Frequency

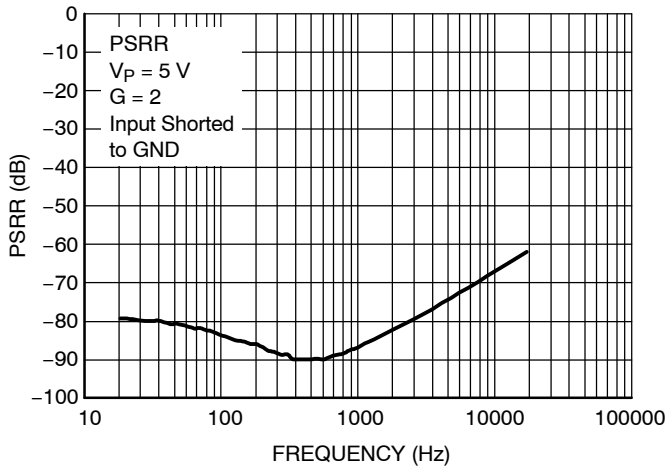


Figure 21. PSRR vs. Frequency

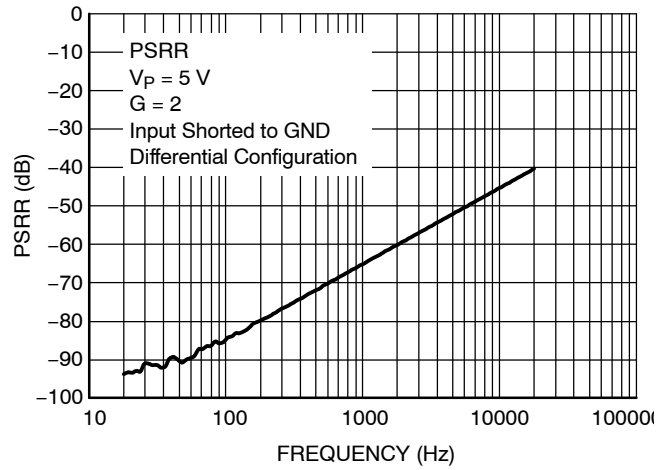


Figure 22. PSRR vs. Frequency

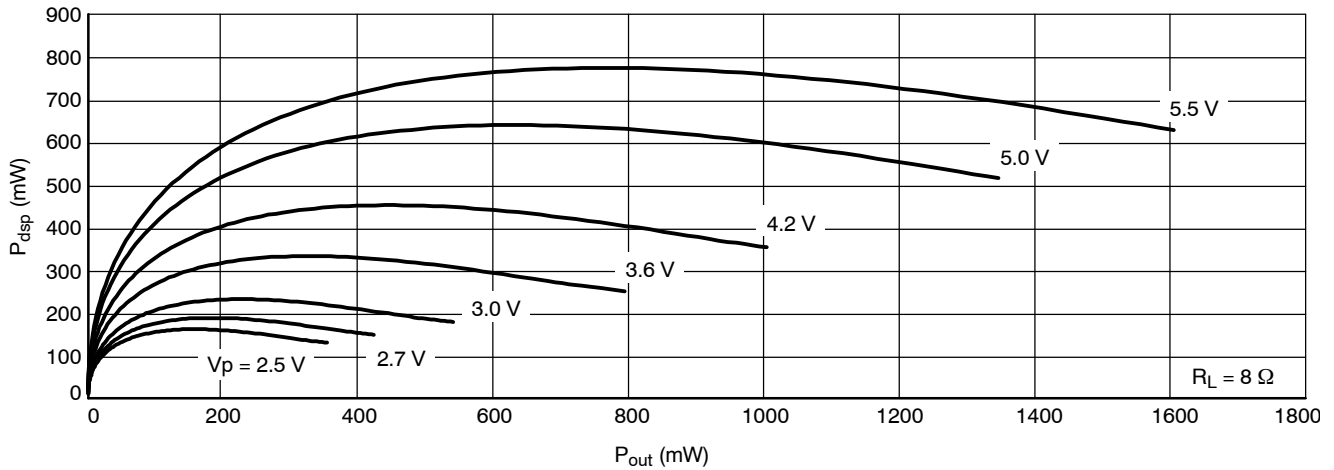


Figure 23. Power Dissipation vs.  $P_{out}$



# NCP2993

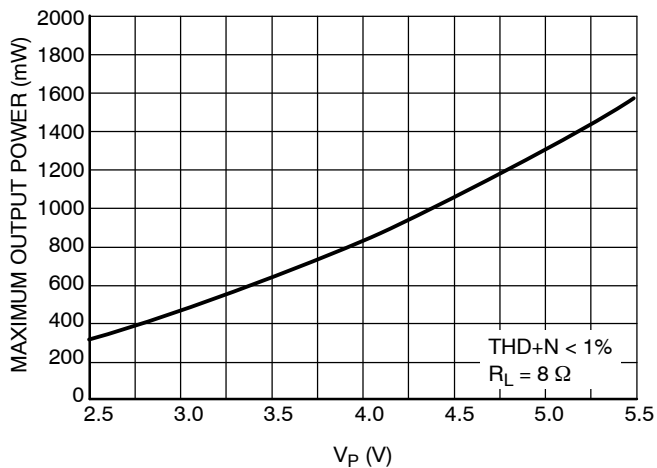


Figure 24. Maximum Output Power vs. V<sub>P</sub>

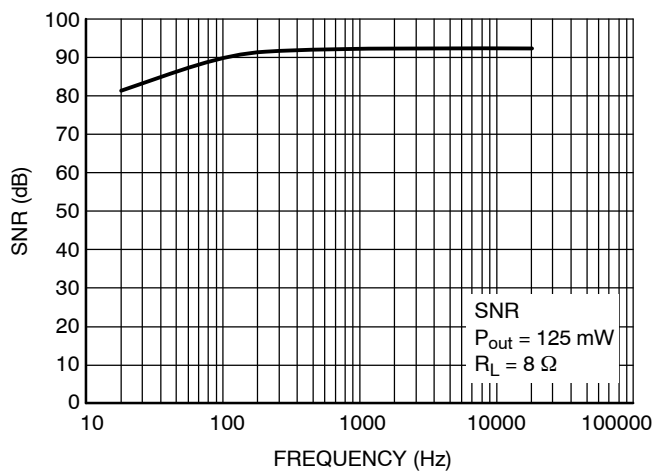


Figure 25. SNR vs. Frequency

## APPLICATION INFORMATION

**Detailed Description**

The NCP2993 audio amplifier can operate under 2.5 V until 5.5 V power supply. With less than 1% THD + N, it can deliver up to 1.35 W RMS output power to an 8.0  $\Omega$  load ( $V_P = 5.0$  V). If application allows to reach 10% THD + N, then 1.65 W can be provided using a 5.0 V power supply.

The structure of the NCP2993 is basically composed of two identical internal power amplifiers; the first one is externally configurable with gain-setting resistors  $R_{in}$  and  $R_f$  (the closed-loop gain is fixed by the ratios of these resistors) and the second is internally fixed in an inverting unity-gain configuration by two resistors of 20 k $\Omega$ . So the load is driven differentially through OUTA and OUTB outputs. This configuration eliminates the need for an output coupling capacitor.

**Internal Power Amplifier**

The output PMOS and NMOS transistors of the amplifier were designed to deliver the output power of the specifications without clipping. The channel resistance ( $R_{on}$ ) of the NMOS and PMOS transistors does not exceed 0.6  $\Omega$  when they drive current.

The structure of the internal power amplifier is composed of three symmetrical gain stages, first and medium gain stages are transconductance gain stages to obtain maximum bandwidth and DC gain.

**Turn-On and Turn-Off Transitions**

When a shutdown low level is applied, the output level is tied to Ground on each output after 10  $\mu$ s.

With  $T_{ON} = GND$ , turn on time is set to 30 ms. With  $T_{ON} = V_P$ , turn on time is set to 15 ms. To avoid any pop and click noises,  $R_{in} * C_{in} < 2.4$  ms with  $T_{ON} = GND$  and  $R_{in} * C_{in} < 1.2$  ms with  $T_{ON} = V_P$ . The electrical characteristics are identical with the 2 configurations. This fast turn on time added to a very low shutdown current saves battery life and brings flexibility when designing the audio section of the final application.

NCP2993 is a zero pop noise device when using a single-ended or differential audio input configuration.

**Shutdown Function**

The device enters shutdown mode when shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 100 nA. In this configuration, the output impedance is 8.5 k $\Omega$  on each output.

**Current Limit Circuit**

The maximum output power of the circuit ( $P_{orms} = 1.0$  W,  $V_P = 5.0$  V,  $R_L = 8.0$   $\Omega$ ) requires a peak current in the load of 500 mA.

In order to limit the excessive power dissipation in the load when a short-circuit occurs, the current limit in the load is fixed to 1.1 A. The current in the four output MOS

transistors are real-time controlled, and when one current exceeds 1.1 A, the gate voltage of the MOS transistor is clipped and no more current can be delivered.

**Thermal Overload Protection**

Internal amplifiers are switched off when the temperature exceeds 160°C, and will be switched on again only when the temperature decreases fewer than 140°C.

The NCP2993 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor and a proper bypassing capacitor in the typical application.

The first amplifier is externally configurable ( $R_f$  and  $R_{in}$ ), while the second is fixed in an inverting unity gain configuration.

The differential-ended amplifier presents two major advantages:

- The possible output power is four times larger (the output swing is doubled) as compared to a single-ended amplifier under the same conditions.
- Output pins (OUTA and OUTB) are biased at the same potential  $V_P/2$ , this eliminates the need for an output coupling capacitor required with a single-ended amplifier configuration.

The differential closed loop-gain of the amplifier is given by  $A_{vd} = 2 * \frac{R_f}{R_{in}} = \frac{V_{orms}}{V_{inrms}}$ .

Output power delivered to the load is given by  $P_{orms} = \frac{(V_{opeak})^2}{2 * R_L}$  ( $V_{opeak}$  is the peak differential output voltage).

When choosing gain configuration to obtain the desired output power, check that the amplifier is not current limited or clipped.

The maximum current which can be delivered to the load is 500 mA  $I_{opeak} = \frac{V_{opeak}}{R_L}$ .

**Gain-Setting Resistor Selection ( $R_{in}$  and  $R_f$ )**

$R_{in}$  and  $R_f$  set the closed-loop gain of the amplifier.

In order to optimize device and system performance, the NCP2993 should be used in low gain configurations.

The low gain configuration minimizes THD + noise values and maximizes the signal to noise ratio, and the amplifier can still be used without running into the bandwidth limitations.

A closed loop gain in the range from 2 to 5 is recommended to optimize overall system performance.

An input resistor ( $R_{in}$ ) value of 24 k $\Omega$  is realistic in most of applications, and doesn't require the use of a too large capacitor  $C_{in}$ .

**Input Capacitor Selection ( $C_{in}$ )**

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a

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high-pass filter with  $R_{in}$ , the cut-off frequency is given by

$$f_c = \frac{1}{2 * \pi * R_{in} * C_{in}}$$

The size of the capacitor must be large enough to couple in low frequencies without severe attenuation.

### IEC 61000-4-2 Level 4

In some particular applications, NCP2993 may need extra ESD protection to pass IEC 61000-4-2 Level 4 qualification.

Depending on the test, user can consider different level of protection:

- up to 22 pF capacitor connected between each amplifier output terminals and ground.
- Dedicated IEC filters such as ESD7.0 series from ON Semiconductor.

In any case, the protection should be placed as close as possible to the ESD stress entry point. Proper and carefull layout is a key factor to ensure optimum protection level is achieved. Designer should make sure the connection impedance between protection and ground / protection and NCP2993 is as low as possible.

### ORDERING INFORMATION

Device	Package	Shipping†
NCP2993FCT2G	9-Pin Flip-Chip (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

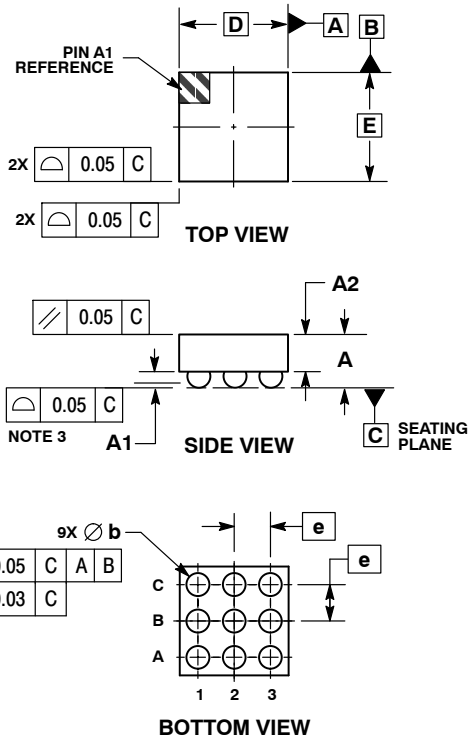
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SCALE 4:1

WLCSP9, 1.22x1.22  
CASE 499BM-01  
ISSUE O

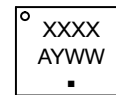
DATE 27 SEP 2010



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.66
A1	0.17	0.24
A2	0.40 REF	
b	0.24	0.29
D	1.22 BSC	
E	1.22 BSC	
e	0.40 BSC	

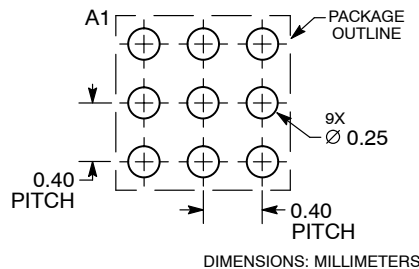
### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON53177E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>WLCSP9, 1.22X1.22</b>	<b>PAGE 1 OF 1</b>

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