

2.5 V / 3.3 V Dual Channel Programmable Clock/Data Delay with Differential CML Outputs

Multi-Level Inputs w/ Internal Termination **NB6L295M**

The NB6L295M is a Dual Channel Programmable Delay Chip designed primarily for Clock or Data de-skewing and timing adjustment. The NB6L295M is versatile in that two individual variable delay channels, PD0 and PD1, can be configured in one of two operating modes, a Dual Delay or an Extended Delay.

In the Dual Delay Mode, each channel has a programmable delay section which is designed using a matrix of gates and a chain of multiplexers. There is a fixed minimum delay of 3.2 ns per channel.

The Extended Delay Mode amounts to the additive delay of PD0 plus PD1 and is accomplished with the Serial Data Interface MSEL bit set High. This will internally cascade the output of PD0 into the input of PD1. Therefore, the Extended Delay path starts at the IN0/IN0 inputs, flows through PD0, cascades to the PD1 and outputs through Q1/Q1. There is a fixed minimum delay of 6.0 ns for the Extended Delay Mode.

The required delay is accomplished by programming each delay channel via a 3-pin Serial Data Interface, described in the application section. The digitally selectable delay has an increment resolution of typically 11 ps with a net programmable delay range of either 0 ns to 6 ns per channel in Dual Delay Mode; or from 0 ns to 11.2 ns for the Extended Delay Mode.

The Multi-Level Inputs can be driven directly by differential LVPECL, LVDS or CML logic levels; or by single ended LVPECL, LVCMOS or LVTTL. A single enable pin is available to control both inputs. The SDI input pins are controlled by LVCMOS or LVTTL level signals. The NB6L295M 16 mA CML output contains temperature compensation circuitry. This device is offered in a 4 mm x 4 mm 24-pin QFN Pb-free package. The NB6L295M is a member of the ECLinPS MAX™ family of high performance products.

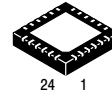
Features

- Input Clock Frequency > 1.5 GHz with 210 mV V_{OUTPP}
- Input Data Rate > 2.5 Gb/s
- Programmable Delay Range: 0 ns to 6 ns per Delay Channel
- Programmable Delay Range: 0 ns to 11.2 ns for Extended Delay Mode
- Total Delay Range: 3.2 ns to 8.5 ns per Delay Channel
- Total Delay Range: 6.2 ns to 16.6 ns in Extended Delay Mode
- Monotonic Delay: 11 ps Increments in 511 Steps
- Linearity ± 20 ps, Maximum
- 100 ps Typical Rise and Fall Times

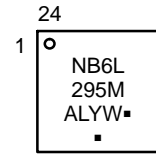
- 2.4 ps Typical Clock Jitter, RMS
- 20 ps Pk-Pk Typical Data Dependent Jitter
- LVPECL, CML or LVDS Differential Input Compatible
- LVPECL, LVCMOS, LVTTL Single Ended Input Compatible
- 3-Wire Serial Interface
- Input Enable/Disable
- Operating Range: $V_{CC} = 2.375$ V to 3.6 V
- CML Output Level; 380 mV Peak-to-Peak, Typical
- Internal 50 Ω Input/Output Termination Provided
- -40°C to 85°C Ambient Operating Temperature
- 24-Pin QFN, 4 mm x 4 mm
- These are Pb-Free Devices*

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAM*



QFN-24
 MN SUFFIX
 CASE 485L



- A = Assembly Location
 - L = Wafer Lot
 - Y = Year
 - W = Work Week
 - = Pb-Free Package
- (Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

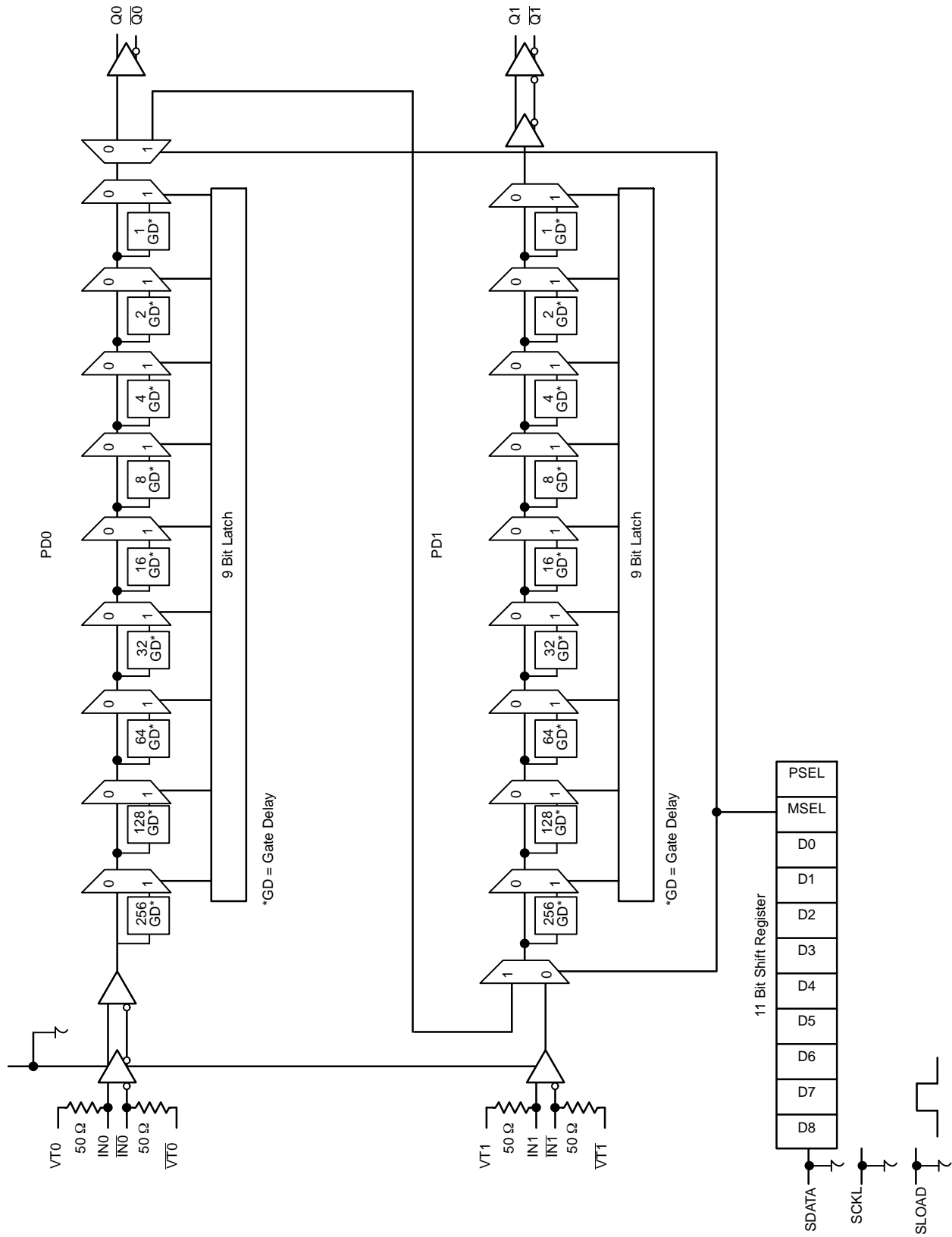


Figure 1. Simplified Functional Block Diagram

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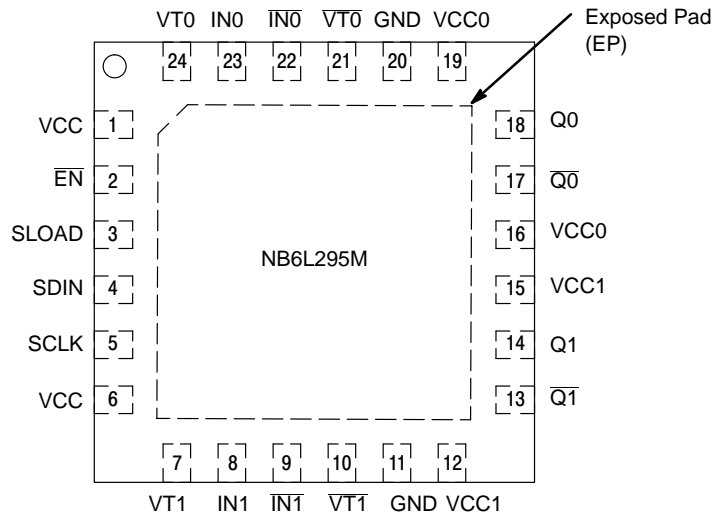


Figure 2. Pinout: QFN-24 (Top View)

Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|-----|-------|-------------------------|--|
| 1 | VCC | Power Supply | Positive Supply Voltage for the Inputs and Core Logic |
| 2 | EN | LVC MOS/LVTTL Input | Input Enable/ Disable for both PD0 and PD1. LOW for enable, HIGH for disable, Open Pin Default state LOW (37 kΩ Pulldown Resistor). High Forces Q LOW and Q HIGH. |
| 3 | SLOAD | LVC MOS/LVTTL Input | Serial Load; This pin loads the configuration latches with the contents of the shift register. The latches will be transparent when this signal is HIGH; thus, the data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation. Open Pin Default state LOW (37 kΩ Pulldown Resistor). |
| 4 | SDIN | LVC MOS/LVTTL Input | Serial Data In; This pin acts as the data input to the serial configuration shift register. Open Pin Default state LOW (37 kΩ Pulldown Resistor). |
| 5 | SCLK | LVC MOS/LVTTL Input | Serial Clock In; This pin serves to clock the serial configuration shift register. Data from SDIN is sampled on the rising edge. Open Pin Default state LOW (37 kΩ Pulldown Resistor). |
| 6 | VCC | Power Supply | Positive Supply Voltage for the Inputs and Core Logic |
| 7 | VT1 | | Internal 50 Ω Termination Pin for IN1. |
| 8 | IN1 | LVPECL, CML, LVDS Input | Noninverted differential input. Note 1. Channel 1. |
| 9 | IN1 | LVPECL, CML, LVDS Input | Inverted differential input. Note 1. Channel 1. |
| 10 | VT1 | | Internal 50 Ω Termination Pin for IN1 |
| 11 | GND | Power Supply | Negative Power Supply |
| 12 | VCC1 | Power Supply | Positive Supply Voltage for the Q1/Q1 outputs, channel PD1 |
| 13 | Q1 | CML Output | Inverted Differential Output. Channel 1. Typically terminated with 50 Ω resistor to VCC1 |
| 14 | Q1 | CML Output | Noninverted Differential Output. Channel 1. Typically terminated with 50 Ω resistor to VCC1 |
| 15 | VCC1 | Power Supply | Positive Supply Voltage for the Q1/Q1 outputs, channel PD1 |
| 16 | VCC0 | Power Supply | Positive Supply Voltage for the Q0/Q0 outputs, channel PD0 |
| 17 | Q0 | CML Output | Inverted Differential Output. Channel 0. Typically terminated with 50 Ω resistor to VCC0 |
| 18 | Q0 | CML Output | Noninverted Differential Output. Channel 0. Typically terminated with 50 Ω resistor to VCC0 |
| 19 | VCC0 | Power Supply | Positive Supply Voltage for the Q0/Q0 outputs, channel PD0 |
| 20 | GND | Power Supply | Negative Power Supply |
| 21 | VT0 | | Internal 50 Ω Termination Pin for IN0 |
| 22 | IN0 | LVPECL, CML, LVDS Input | Inverted differential input. Note 1. Channel 0. |
| 23 | IN0 | LVPECL, CML, LVDS Input | Noninverted differential input. Note 1. Channel 0. |
| 24 | VT0 | | Internal 50 Ω Termination Pin for IN0 |
| - | EP | Ground | The Exposed Pad (EP) on the QFN-24 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to GND and must be connected to GND on the PC board. |

1. In the differential configuration when the input termination pin (VTx/VTx) are connected to a common termination voltage or left open, and if no signal is applied on INx/INx input then the device will be susceptible to self-oscillation.
2. All VCC, VCC0 and VCC1 Pins must be externally connected to the same power supply for proper operation. Both VCC0s are connected to each other and both VCC1s are connected to each other: VCC0 and VCC1 are separate.

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Table 2. ATTRIBUTES

| Characteristics | | Value |
|--|-----------------------------------|----------------------|
| Input Default State Resistors | | 37 kΩ |
| ESD Protection | Human Body Model Machine Model | > 2 kV > 100V |
| Moisture Sensitivity (Note 3) | QFN-24 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | | 3094 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

3. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|----------------------------|---|--------------------|--------------------------------------|----------------|--------------|
| V_{CC}, V_{CC0}, V_{CC1} | Positive Power Supply | GND = 0 V | | 4.0 | V |
| V_{IO} | Positive Input/Output Voltage | GND = 0 V | $-0.5 \leq V_{IO} \leq V_{CC} + 0.5$ | 4.5 | V |
| V_{INPP} | Differential Input Voltage $ I_{Nx} - \overline{I_{Nx}} $ | | | $V_{CC} - GND$ | V |
| I_{IN} | Input Current Through R_T (50 Ω Resistor) | | | ± 50 | mA |
| I_{OUT} | Output Current Through R_T (50 Ω Resistor) | | | ± 50 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | °C |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) (Note 4) | 0 lfpm 500 lfpm | QFN-24 QFN-24 | 37 32 | °C/W °C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | (Note 4) | QFN-24 | 11 | °C/W |
| T_{sol} | Wave Solder Pb-Free | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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Table 4. DC CHARACTERISTICS, MULTI-LEVEL INPUTS $V_{CC} = V_{CC0} = V_{CC1} = 2.375\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--------|----------------|-----|-----|-----|------|
|--------|----------------|-----|-----|-----|------|

POWER SUPPLY CURRENT

| | | | | | |
|----------|---|--|-----|-----|----|
| I_{CC} | Power Supply Current (Inputs, V_{TX} and Outputs Open) (Sum of I_{CC} , I_{CC0} , and I_{CC1}) | | 170 | 215 | mA |
|----------|---|--|-----|-----|----|

CML OUTPUTS (Notes 5 and 6, Figure 22)

| | | | | | |
|----------|---|--------------------------------|--------------------------------|--------------------------------|----|
| V_{OH} | Output HIGH Voltage $V_{CC} = V_{CC0} = V_{CC1} = 3.3\text{ V}$ $V_{CC} = V_{CC0} = V_{CC1} = 2.5\text{ V}$ | $V_{CC} - 40$ 3260 2460 | $V_{CC} - 10$ 3290 2490 | V_{CC} 3300 2500 | mV |
| V_{OL} | Output LOW Voltage $V_{CC} = V_{CC0} = V_{CC1} = 3.3\text{ V}$ $V_{CC} = V_{CC0} = V_{CC1} = 2.5\text{ V}$ | $V_{CC} - 500$ 2800 2000 | $V_{CC} - 400$ 2900 2100 | $V_{CC} - 300$ 3000 2200 | mV |

DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (see Figures 11 and 12) (Note 7)

| | | | | | |
|-----------|--|----------------|--|----------------|----|
| V_{th} | Input Threshold Reference Voltage Range | 1050 | | $V_{CC} - 150$ | mV |
| V_{IH} | Single-Ended Input HIGH Voltage | $V_{th} + 150$ | | V_{CC} | mV |
| V_{IL} | Single-Ended Input LOW Voltage | GND | | $V_{th} - 150$ | mV |
| V_{ISE} | Single-Ended Input Voltage Amplitude ($V_{IH} - V_{IL}$) | 300 | | $V_{CC} - GND$ | mV |

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 13 and 14) (Note 8)

| | | | | | |
|-----------|---|------|--|----------------|---------------|
| V_{IHD} | Differential Input HIGH Voltage | 1200 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | GND | | $V_{CC} - 150$ | mV |
| V_{ID} | Differential Input Voltage Swing ($I_{NX}/\overline{I_{NX}}$) ($V_{IHD} - V_{ILD}$) | 150 | | $V_{CC} - GND$ | mV |
| V_{CMR} | Input Common Mode Range (Differential Configuration) (Note 9) | 950 | | $V_{CC} - 75$ | mV |
| I_{IH} | Input HIGH Current $I_{NX}/\overline{I_{NX}}$, (V_{Tn}/\sqrt{Tn} Open) | -150 | | 150 | μA |
| I_{IL} | Input LOW Current $I_{NX}/\overline{I_{NX}}$, (V_{Tn}/\sqrt{Tn} Open) | -150 | | 150 | μA |

SINGLE-ENDED LVCMOS/LVTTL CONTROL INPUTS

| | | | | | |
|----------|---------------------------------|------|--|----------|---------------|
| V_{IH} | Single-Ended Input HIGH Voltage | 2000 | | V_{CC} | mV |
| V_{IL} | Single-Ended Input LOW Voltage | GND | | 800 | mV |
| I_{IH} | Input HIGH Current | -150 | | 150 | μA |
| I_{IL} | Input LOW Current | -150 | | 150 | μA |

TERMINATION RESISTORS

| | | | | | |
|------------|--------------------------------------|----|----|----|----------|
| R_{TIN} | Internal Input Termination Resistor | 40 | 50 | 60 | Ω |
| R_{TOUT} | Internal Output Termination Resistor | 40 | 50 | 60 | Ω |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

- CML outputs loaded with $50\ \Omega$ to V_{CC} for proper operation.
- Input and output parameters vary 1:1 with V_{CC} .
- V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously. V_{th} is applied to the complementary input when operating in single-ended mode.
- V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
- $V_{CMR}(\text{min})$ varies 1:1 with voltage on GND pin, $V_{CMR}(\text{max})$ varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

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Table 5. AC CHARACTERISTICS $V_{CC} = V_{CC0} = V_{CC1} = 2.375 \text{ V to } 3.6 \text{ V}$, $GND = 0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ (Note 10)

| Symbol | Characteristic | Min | | | Typ | | | Max | | | Unit |
|--|--|------------|------------|------------|------------|--|------------|--|------------|-------------|------|
| f _{SCLK} | Serial Clock Input Frequency, 50% Duty Cycle | | | | | | | 20 | | | MHz |
| V _{OUTPP} | Output Voltage Amplitude (@ V _{INPPmin}) f _{in} ≤ 1.5 GHz (Note 15) (See Figure 23) | 210 | | | 380 | | | | | | mV |
| f _{DATA} | Maximum Data Rate (Note 14) | 2.5 | | | | | | | | | Gb/s |
| t _{Range} | Programmable Delay Range (@ 50 MHz) Dual Mode IN0/IN0 to Q0/Q0 or IN1/IN1 to Q1/Q1 Extended Mode IN0/IN0 to Q1/Q1 | 0 | | | 5.7 | | | 6.9 | | | ns |
| t _{SKEW} | Duty Cycle Skew (Note 11) Within Device Skew – Dual Mode D[8:0] = 0 D[8:0] = 1 | 0 | | | 1 | | | 4 | | | ps |
| L _{in} | Linearity (Note 12) | | | | ± 15 | | | ± 20 | | | ps |
| t _s | Setup Time (@ 20 MHz) SDIN to SCLK SCLK to SLOAD EN to SDIN | 0.5 | | | 0.3 | | | | | | ns |
| t _h | Hold Time SDIN to SCLK SCLK to SLOAD EN to SLOAD | 1.0 | | | 0.6 | | | | | | ns |
| t _{pwmin} | Minimum Pulse Width SLOAD | 1 | | | | | | | | | ns |
| t _{JITTER} | Random Clock Jitter RMS; SETMIN to SETMAX (Note 13) f _{in} ≤ 1.5 GHz Dual Mode IN0/IN0 to Q0/Q0 or IN1/IN1 to Q1/Q1 Extended Mode IN0/IN0 to Q1/Q1 Deterministic Jitter; SETMIN to SETMAX (Note 14) f _{D-ATA} ≤ 2.5 Gbps Dual Mode IN0/IN0 to Q0/Q0 or IN1/IN1 to Q1/Q1 | | | | 2 | | | 6 | | | ps |
| V _{INPP} | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 15) | 150 | | | | | | V _{CC} – GND | | | mV |
| t _r , t _f | Output Rise/Fall Times (@ 50 MHz), (20% – 80%) Qx, Qx | 85 | | | 100 | | | 150 | | | ps |
| Symbol | Characteristic | –40°C | | | +25°C | | | +85°C | | | Unit |
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay (@ 50 MHz) Dual Mode IN0/IN0 to Q0/Q0 or IN1/IN1 to Q1/Q1 D[8:0] = 0 D[8:0] = 1 Extended Mode IN0/IN0 to Q1/Q1 D[8:0] = 0 D[8:0] = 1 | 2.7 7.2 | 3.1 8.5 | 3.3 9.1 | 2.8 7.4 | 3.2 8.5 | 3.5 9.6 | 3.1 8.6 | 3.4 9.3 | 3.8 10.7 | ns |
| Δt | Step Delay (Selected D Bit HIGH All Others LOW) D0 HIGH D1 HIGH D2 HIGH D3 HIGH D4 HIGH D5 HIGH D6 HIGH D7 HIGH D8 HIGH | | | | | 8.4 16.4 41.2 85 178 360 722 1448 2903 | | 12.4 25.1 58.3 108 210 405 796 1579 3143 | | | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

10. Measured by forcing V_{INPPmin} and V_{INPPmax} from a 50% duty cycle clock source, V_{CMR} (min and max). All loading with an external R_L = 50 Ω to V_{CC}. See Figure 20. Input edge rates 40 ps (20% – 80%).

11. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw-} and T_{pw+} @ 0.5 GHz.

12. Deviation from a linear delay (actual Min to Max) in the Dual Mode 511 programmable steps; 3.3 V @ 25°C, 400 mV V_{INPP}.

13. Additive Random CLOCK jitter with 50% duty cycle input clock signal. 1000 WFMS, JIT3 Software.

14. NRZ data at PRBS23 and K28.5. 10,000 WFMS, TDS8000.

15. Input and output voltage swing is a single-ended measurement operating in differential mode.

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Serial Data Interface Programming

The NB6L295M is programmed by loading the 11–Bit SHIFT REGISTER using the SCLK, SDATA and SLOAD inputs. The 11 SDATA bits are 1 PSEL bit, 1 MSEL bit and 9 delay value data bits D[8:0]. A separate 11–bit load cycle is required to program the delay data value of each channel, PD0 and PD1. For example, at powerup two load cycles will be needed to initially set PD0 and PD1; Dual Mode Operation as shown in Figures 3 and 4 and Extended Mode Operation as shown in Figures 5 and 6.

DUAL MODE OPERATIONS

| PD0 Programmable Delay | | | | | | | | | | Control Bits | | |
|------------------------|-----|-----|-----|-----|-----|-----|-----|-----|------|--------------|---|-------------------|
| 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0 | 0 | Value Bit Name |
| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | MSEL | PSEL | | |

(MSB) (LSB)

Figure 3. PDO Shift Register

| PD1 Programmable Delay | | | | | | | | | | Control Bits | | |
|------------------------|-----|-----|-----|-----|-----|-----|-----|-----|------|--------------|---|-------------------|
| 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0 | 1 | Value Bit Name |
| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | MSEL | PSEL | | |

(MSB) (LSB)

Figure 4. PD1 Shift Register

EXTENDED MODE OPERATIONS

| PD0 Programmable Delay | | | | | | | | | | Control Bits | | |
|------------------------|-----|-----|-----|-----|-----|-----|-----|-----|------|--------------|---|-------------------|
| 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 1 | 0 | Value Bit Name |
| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | MSEL | PSEL | | |

(MSB) (LSB)

Figure 5. PDO Shift Register

| PD1 Programmable Delay | | | | | | | | | | Control Bits | | |
|------------------------|-----|-----|-----|-----|-----|-----|-----|-----|------|--------------|---|-------------------|
| 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 1 | 1 | Value Bit Name |
| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | MSEL | PSEL | | |

(MSB) (LSB)

Figure 6. PD1 Shift Register

Refer to Table 6, Channel and Mode Select BIT Functions. In a load cycle, the 11–Bit Shift Register least significant bit (clocked in first) is **PSEL** and will determine which channel delay buffer, either PD0 (LOW) or PD1 (HIGH), will latch the delay data value D[8:0]. The **MSEL BIT** determines the Delay Mode. When set LOW, the Dual Delay Mode is selected and the device uses both channels independently. A pulse edge entering $IN0/\overline{IN0}$ is delayed according to the values in PD0 and exits from $Q0/\overline{Q0}$. An input signal pulse edge entering $IN1/\overline{IN1}$ is delayed according to the values in PD1 and exits from $Q1/\overline{Q1}$. When MSEL is set HIGH, the Extended Delay Mode is selected and an input signal pulse edge enters $IN0$ and $\overline{IN0}$ and flows through PD0 and is extended through PD1 to exit at $Q1$ and $\overline{Q1}$. The most significant 9–bits, D[8:0] are delay value data for both channels. See Figure 7.

Table 6. CHANNEL AND MODE SELECT BIT FUNCTIONS

| BIT Name | Function |
|----------|---|
| PSEL | 0 Loads Data to PD0 |
| | 1 Loads Data to PD1 |
| MSEL | 0 Selects Dual Programmable Delay Paths, 3.1 ns to 8.8 ns Delay Range for Each Path |
| | 1 Selects Extended Delay Path from $IN0/\overline{IN0}$ to $Q1/\overline{Q1}$, 6.0 ns to 17.2 ns Delay Range; Disables $Q0/\overline{Q0}$ Outputs, $Q0$ –LOW, $\overline{Q0}$ –HIGH. |
| D[8:0] | Select one of 512 Delay Values |

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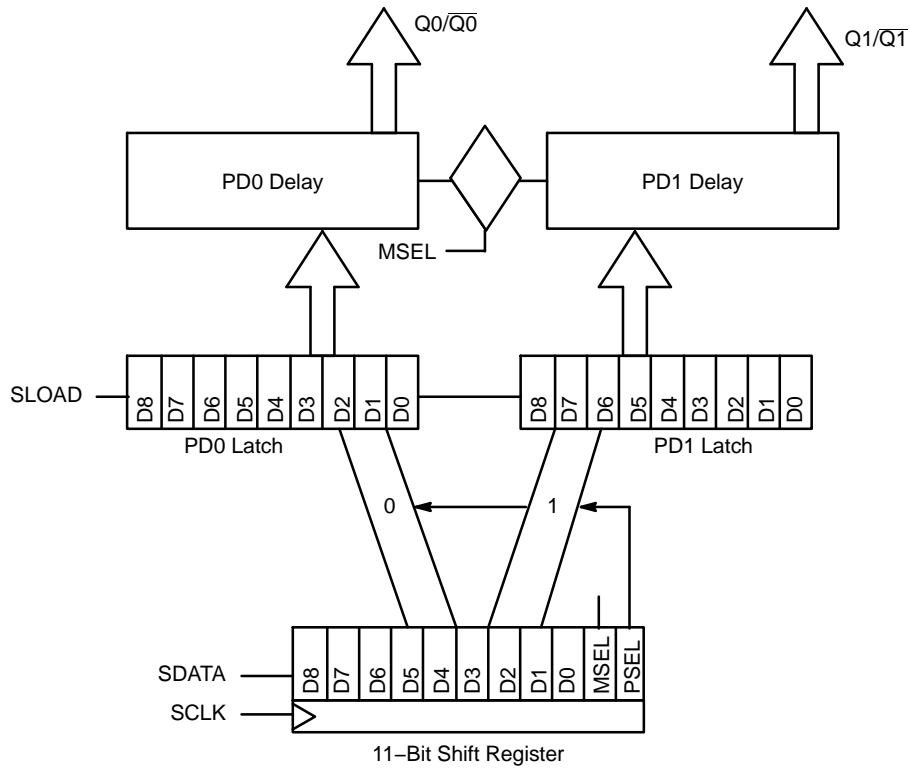


Figure 7. Serial Data Interface, Shift Register, Data Latch, Programmable Delay Channels Load Cycle Required for Each Channel

Serial Data Interface Loading

Loading the device through the 3 input Serial Data Interface (SDI) is accomplished by sending data into the SDIN pin by using the SCLK input pin and latching the data with the SLOAD input pin. The 11-bit SHIFT REGISTER shifts once per rising edge of the SCLK input. The serial input SDIN must meet setup and hold timing as specified in the AC Characteristics section of this document for each bit and clock pulse. The SLOAD line loads the value of the shift register on a LOW-to-HIGH edge transition (transparent state) into a data Latch register and latches the data with a subsequent HIGH-to-LOW edge transition. Further changes in SDIN or SCLK are not recognized by the latched register. The internal multiplexer states are set by the PSEL and MSEL bits in the SHIFT register. Figure 6 shows the timing diagram of a typical load sequence.

Input EN should be LOW (enabled) prior to SDI programming, then pulled HIGH (disabled) during programming. After programming, the EN should be returned LOW (enabled) for functional delay operation.

The disabling of EN (HIGH) forces Qx LOW and Qx HIGH and is included during programming to prevent (or mask out) any potential run pulses or extended pulses which might occur in the internal delay gates programming switching, but it is not required for programming.

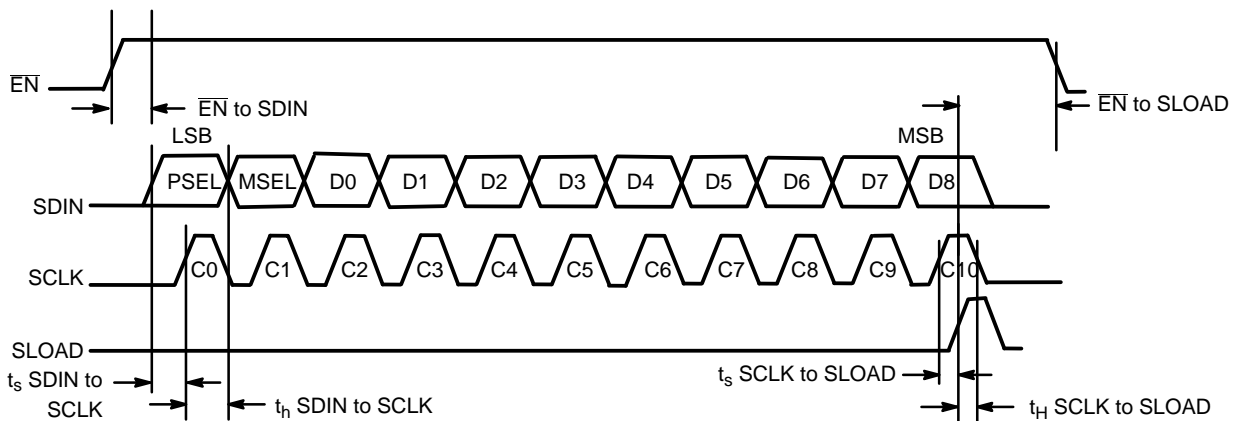


Figure 8. SDI Programming Cycle Timing Diagram (Load Cycle 1 of 2)

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Table 7 shows theoretical values of delay capabilities in both the Dual Delay Mode and in the Extended Delay Modes of operation.

Table 7. EXAMPLES OF THEORETICAL DELAY VALUES FOR PD0 AND PD1 IN DUAL MODE

INPUTS: IN0/IN $\bar{0}$, IN1/IN $\bar{1}$, OUTPUTS: Q0/Q $\bar{0}$, Q1, Q $\bar{1}$

| Dual Mode | | | | PD0 Delay* (ps) | PD1 Delay* (ps) |
|------------|-----------|-------------|-----------|-----------------|-----------------|
| PD1 D[8:0] | (Decimal) | PD0 D[8:0] | (Decimal) | | |
| 00000000 | (0) | 00000000 | (0) | 0 | 0 |
| 00000000 | (0) | 00000001 | (1) | 0 | 11 |
| 00000000 | (0) | 00000010 | (2) | 0 | 22 |
| 00000000 | (0) | 00000011 | (3) | 0 | 33 |
| 00000000 | (0) | 00000100 | (4) | 0 | 44 |
| 00000000 | (0) | 00000101 | (5) | 0 | 55 |
| 00000000 | (0) | 00000110 | (6) | 0 | 66 |
| 00000000 | (0) | 00000111 | (7) | 0 | 77 |
| 00000000 | (0) | 00001000 | (8) | 0 | 88 |
| | | • • • | | • • • | • • • |
| 00000000 | (0) | 00001000 | (16) | 0 | 176 |
| 00000000 | (0) | 00010000 | (32) | 0 | 352 |
| 00000000 | (0) | 00100000 | (64) | 0 | 704 |
| 00000000 | (0) | 11111101 | (509) | 0 | 5599 |
| 00000000 | (0) | 11111110 | (510) | 0 | 5610 |
| 00000000 | (0) | 11111111 | (511) | 0 | 5621 |

*Fixed minimum delay not included

Table 8. EXAMPLES OF THEORETICAL DELAY VALUES FOR PD0 AND PD1 IN EXTENDED MODE

INPUTS: IN0/IN $\bar{0}$, IN1/IN $\bar{1}$, OUTPUTS: Q0/Q $\bar{0}$, Q1, Q $\bar{1}$

| Extended Delay Mode | | | | PD0* (ps) | PD1* (ps) | Total Delay* (ps) |
|---------------------|-----------|-------------|-----------|-----------|-------------|-------------------|
| PD1 D[8:0] | (Decimal) | PD0 D[8:0] | (Decimal) | | | |
| 00000000 | (0) | 00000000 | (0) | 1 | 0 | 0 |
| 00000000 | (0) | 00000001 | (1) | 1 | 0 | 11 |
| 00000000 | (0) | 00000010 | (2) | 1 | 0 | 22 |
| 00000000 | (0) | 00000011 | (3) | 1 | 0 | 33 |
| | | • • • | | | • • • | • • • |
| 00000000 | (0) | 11111101 | (509) | 1 | 0 | 5599 |
| 00000000 | (0) | 11111110 | (510) | 1 | 0 | 5610 |
| 00000000 | (0) | 11111111 | (511) | 1 | 0 | 5621 |
| 00000001 | (1) | 11111111 | (511) | 1 | 11 | 5632 |
| 00000010 | (2) | 11111111 | (511) | 1 | 22 | 5643 |
| | | • • • | | | • • • | • • • |
| 11111100 | (508) | 11111111 | (511) | 1 | 5588 | 5621 |
| 11111101 | (509) | 11111111 | (511) | 1 | 5599 | 5621 |
| 11111110 | (510) | 11111111 | (511) | 1 | 5610 | 5621 |
| 11111111 | (511) | 11111111 | (511) | 1 | 5621 | 5621 |

*Fixed minimum delay not included

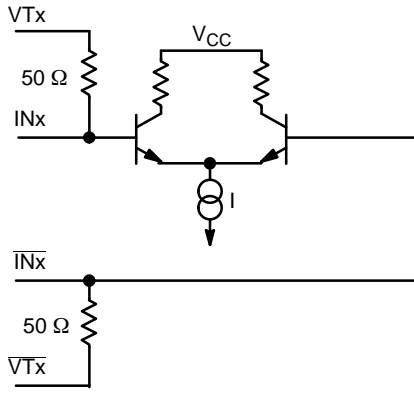


Figure 9. Input Structure

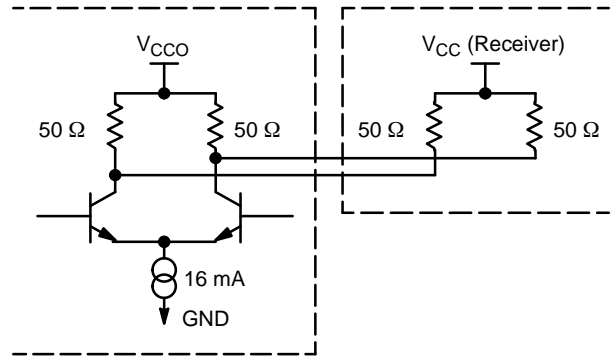


Figure 10. Typical CML Output Structure and Termination

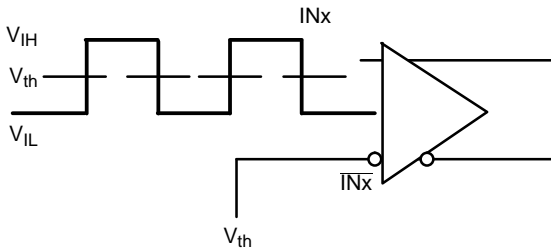


Figure 11. Differential Input Driven Single-Ended

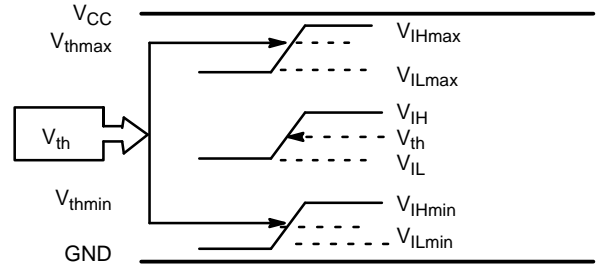


Figure 12. V_{th} Diagram

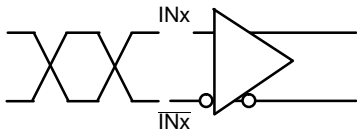


Figure 13. Differential Inputs Driven Differentially

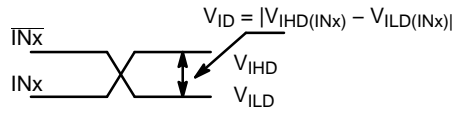


Figure 14. Differential Inputs Driven Differentially

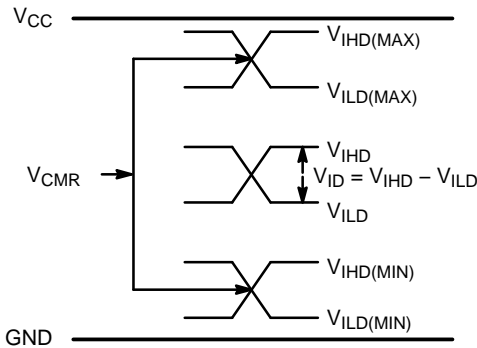


Figure 15. V_{CMR} Diagram

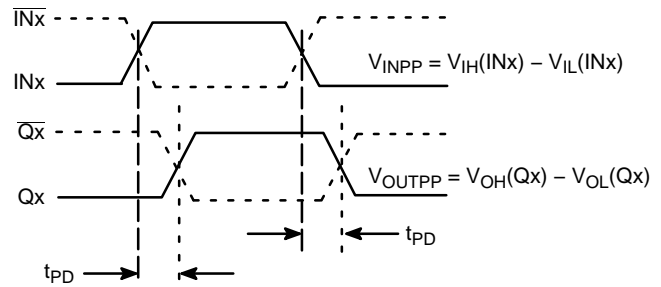


Figure 16. AC Reference Measurement

NB6L295M

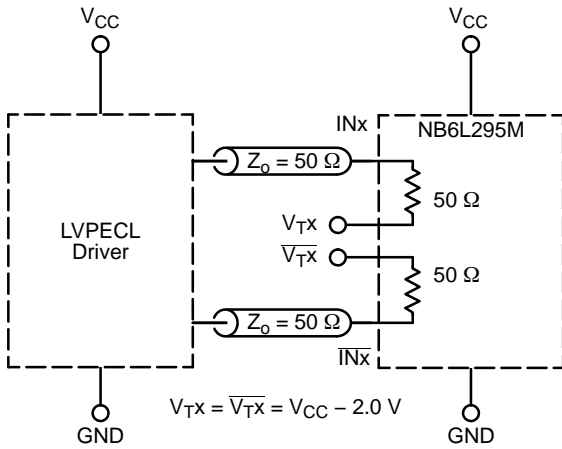


Figure 17. LVPECL Interface

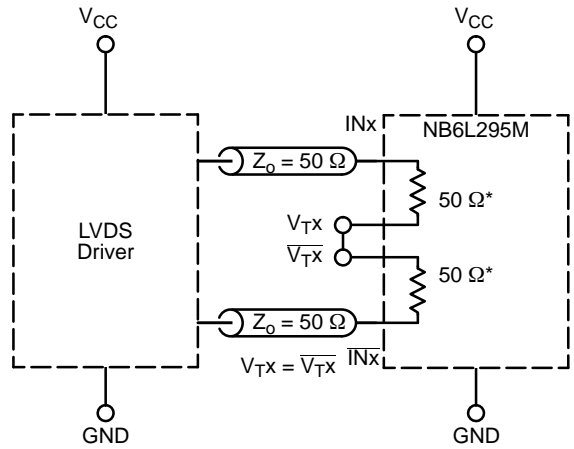


Figure 18. LVDS Interface

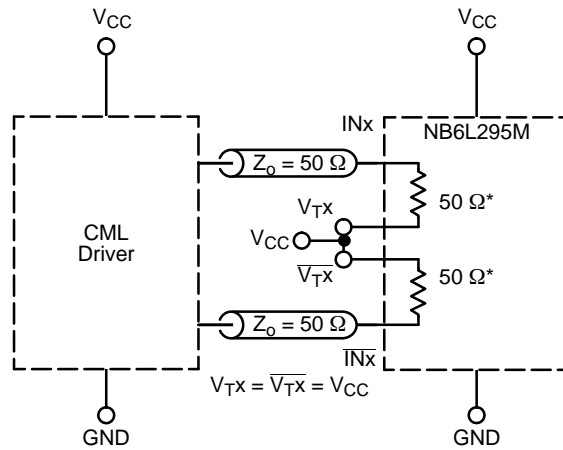


Figure 19. CML Interface, Standard 50 Ω Load

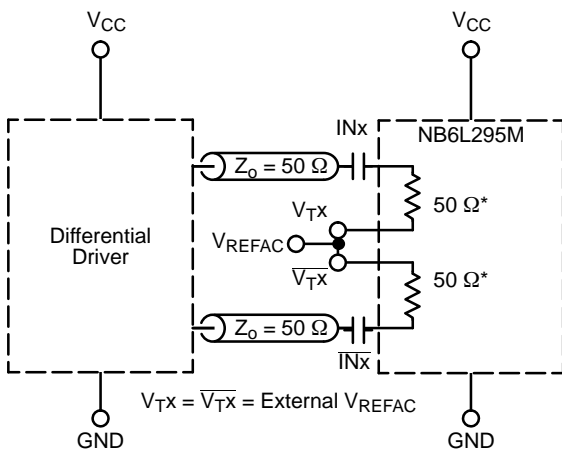


Figure 20. Capacitor-Coupled Differential Interface ($V_{TX}/\overline{V_{TX}}$ Connected to V_{REFAC} ; V_{REFAC} Bypassed to Ground with 0.1 μF Capacitor)

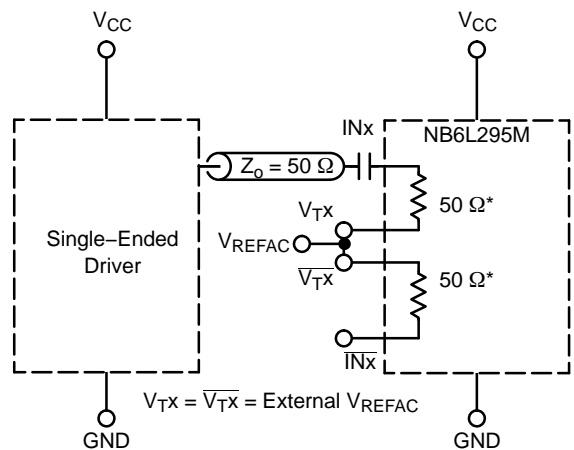


Figure 21. Capacitor-Coupled Single-Ended Interface ($V_{TX}/\overline{V_{TX}}$ Connected to External V_{REFAC} ; V_{REFAC} Bypassed to Ground with 0.1 μF Capacitor)

NB6L295M

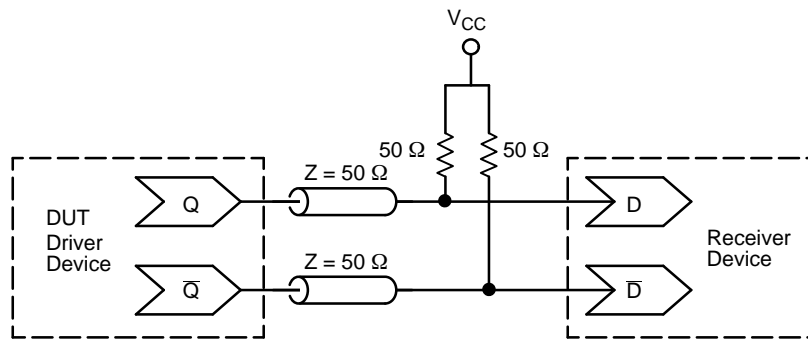


Figure 22. Typical Termination for Output Driver and Device Evaluation

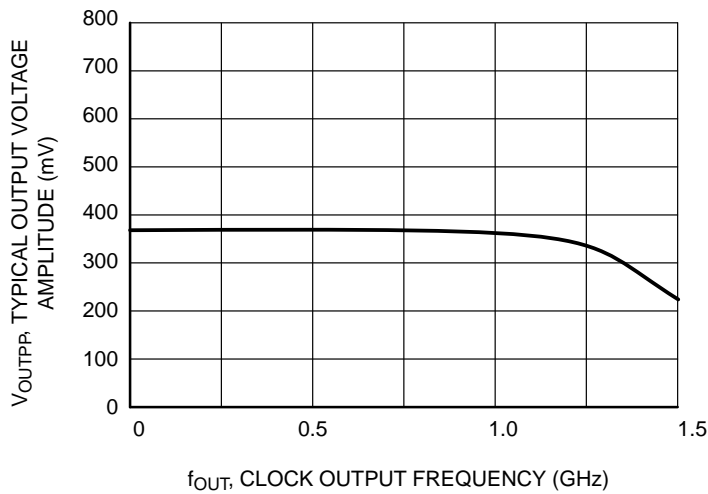


Figure 23. Output Voltage Amplitude (V_{OUTPP}) vs. Output Frequency at Ambient Temperature (Typical)

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|---------------|---------------------|-----------------------|
| NB6L295MMNG | QFN-24 (Pb-free) | 92 Units / Rail |
| NB6L295MMNTXG | QFN-24 (Pb-free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

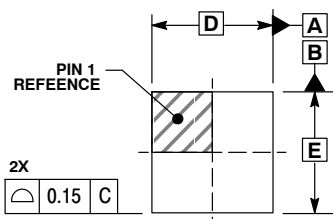


1 24

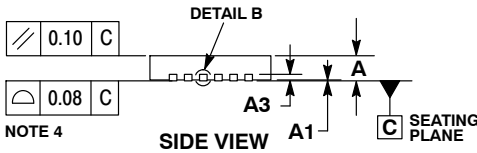
SCALE 2:1

QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

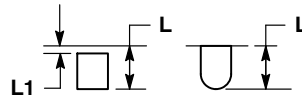
DATE 05 JUN 2012



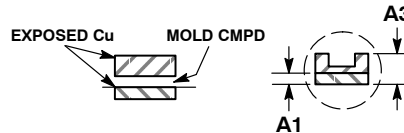
TOP VIEW



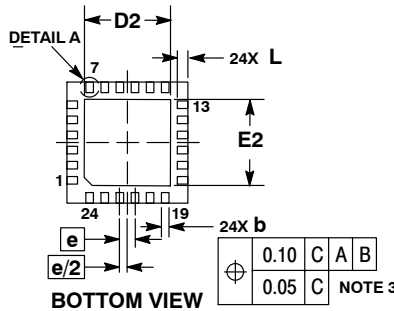
SIDE VIEW



DETAIL A
ALTERNATE
CONSTRUCTIONS



DETAIL B
ALTERNATE TERMINAL
CONSTRUCTIONS



BOTTOM VIEW

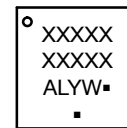
| | | | |
|------|---|--------|---|
| 0.10 | C | A | B |
| 0.05 | C | NOTE 3 | |

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
- COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.20 | 0.30 |
| D | 4.00 | BSC |
| D2 | 2.70 | 2.90 |
| E | 4.00 | BSC |
| E2 | 2.70 | 2.90 |
| e | 0.50 | BSC |
| L | 0.30 | 0.50 |
| L1 | 0.05 | 0.15 |

GENERIC MARKING DIAGRAM*

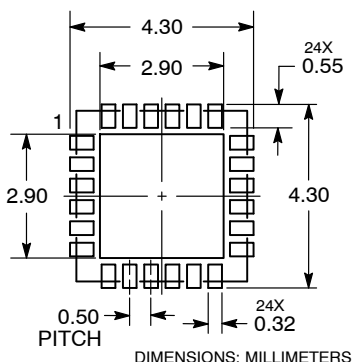


- XXXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

| | | |
|------------------|------------------|--|
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| DESCRIPTION: | QFN24, 4X4, 0.5P | PAGE 1 OF 1 |

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