

AC/DC to Logic Interface Optocoupler

HCPL3700M

Description

The HCPL3700M voltage/current threshold detection optocoupler consists of an AlGaAs LED connected to a threshold sensing input buffer IC which are optically coupled to a high gain darlington output. The input buffer chip is capable of controlling threshold levels over a wide range of input voltages with a single resistor. The output is TTL and CMOS compatible.

Features

- AC or DC Input
- Programmable Sense Voltage
- Logic Level Compatibility
- Threshold Guaranteed Over Temperature (0°C to 70°C)
- Safety and Regulatory Approvals
 - ◆ UL1577, 5,000 VAC_{RMS} for 1 Minute
 - ◆ DIN EN/IEC60747-5-5
- These are Pb-Free Devices

Applications

- Low Voltage Detection
- 5 V to 240 V AC/DC Voltage Sensing
- Relay Contact Monitor
- Current Sensing
- Microprocessor Interface
- Industrial Controls

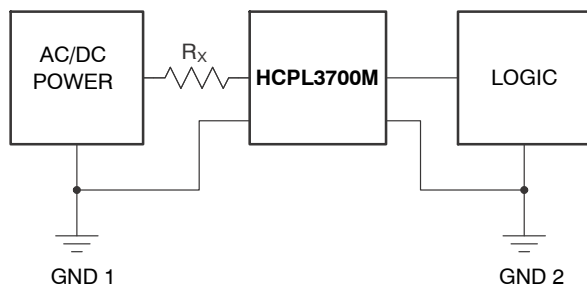
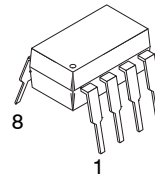
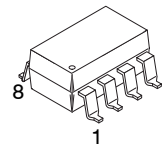


Figure 1. Schematic

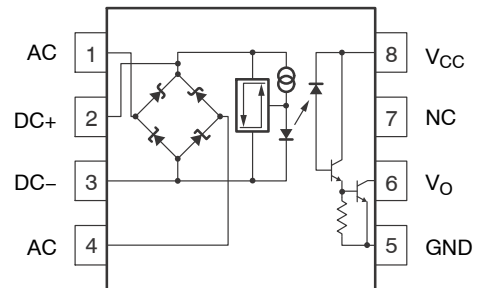


PDIP8 9.655x6.6, 2.54P
CASE 646CQ



PDIP8 GW
CASE 709AC

ELECTRICAL CONNECTION

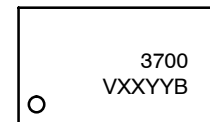


TRUTH TABLE (Positive Logic)

Input	Output
H	L
L	H

A 0.1 μF bypass capacitor must be connected between pins 8 and 5.

MARKING DIAGRAM



- 3700 = Device Number
- V = DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
- XX = Two-Digit Year Code
- YY = Two-Digit Work Week
- B = Assembly Package Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

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SAFETY AND INSULATION RATINGS (As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Parameter	Characteristics	
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	< 150 V _{RMS}	I-IV
	< 300 V _{RMS}	I-IV
	< 450 V _{RMS}	I-III
	< 600 V _{RMS}	I-III
	< 1000 V _{RMS} (Option TV)	I-III
Climatic Classification	40/85/21	
Pollution Degree (DIN VDE 0110/1.89)	2	
Comparative Tracking Index	175	

Symbol	Parameter	Value	Unit
V _{PR}	Input-to-Output Test Voltage, Method A, V _{IORM} × 1.6 = V _{PR} , Type and Sample Test with t _m = 10 s, Partial Discharge < 5 pC	2,262	V _{peak}
	Input-to-Output Test Voltage, Method B, V _{IORM} × 1.875 = V _{PR} , 100% Production Test with t _m = 1 s, Partial Discharge < 5 pC	2,651	V _{peak}
V _{IORM}	Maximum Working Insulation Voltage	1,414	V _{peak}
V _{IOTM}	Highest Allowable Over-Voltage	6,000	V _{peak}
	External Creepage	≥ 8.0	mm
	External Clearance	≥ 7.4	mm
	External Clearance (for Option TV, 0.4" Lead Spacing)	≥ 10.16	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥ 0.5	mm
T _S	Case Temperature (Note 1)	150	°C
I _{S,INPUT}	Input Current (Note 1)	25	mA
P _{S,OUTPUT}	Output Power (Duty Factor ≤ 2.7%) (Note 1)	250	mW
R _{IO}	Insulation Resistance at T _S , V _{IO} = 500 V (Note 1)	> 10 ⁹	Ω

1. Safety limit value – maximum values allowed in the event of a failure.

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Value	Units
T _{STG}	Storage Temperature	-40 to +125	°C
T _{OPR}	Operating Temperature	-40 to +85	°C
T _J	Junction Temperature	-40 to +125	°C
T _{SOL}	Lead Solder Temperature	260 for 10 s	°C
P _T	Total Package Power Dissipation (Note 2)	305	mW

EMITTER

I _{IN}	Input Current	Average	50	mA
		Surge, 3 ms, 120 Hz Pulse Rate	140	
		Transient, 10 μs, 120 Hz Pulse Rate	500	
V _{IN}	Input Voltage (Pins 2-3)		-0.5	V
P _{IN}	Input Power Dissipation (Note 3)		230	mW

DETECTOR

I _O	Output Current (Average) (Note 4)		30	mA
V _{CC}	Supply Voltage (Pins 8-5)		-0.5 to 20	V
V _O	Output Voltage (Pins 6-5)		-0.5 to 20	V
P _O	Output Power Dissipation (Note 5)		210	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Derate linearly above 70°C free-air temperature at a rate of 2.5 mW/°C.
- Derate linearly above 70°C free-air temperature at a rate of 1.8 mW/°C.
- Derate linearly above 70°C free-air temperature at a rate of 0.6 mA/°C.
- Derate linearly above 70°C free-air temperature at a rate of 1.9 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	2	18	V
T _A	Ambient Operating Temperature	0	70	°C
f	Operating Frequency	0	4	kHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C unless otherwise specified)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I _{TH+}	Input Threshold Current		V _{IN} = V _{TH+} , V _{CC} = 4.5 V	1.96	2.40	3.11	mA
I _{TH-}			V _O = 0.4 V, I _O ≥ 4.2 mA (Note 6)	1.00	1.20	1.62	
V _{TH+}	Input Threshold Voltage	DC (Pins 2, 3)	V _{IN} = V ₂ - V ₃ (Pins 1 & 4 Open) V _{CC} = 4.5 V, V _O = 0.4 V (Note 6) I _O ≥ 4.2 mA	3.35	3.80	4.05	V
V _{TH-}			V _{IN} = V ₂ - V ₃ (Pins 1 & 4 Open) V _{CC} = 4.5 V, V _O = 2.4 V (Note 6) I _O ≥ 100 μA	2.01	2.50	2.86	V
V _{TH+}		AC (Pins 1, 4)	V _{IN} = V ₁ - V ₄ (Pins 2 & 3 Open) V _{CC} = 4.5 V, V _O = 0.4 V (Note 6) I _O ≥ 4.2 mA	4.23	5.00	5.50	V
V _{TH-}			V _{IN} = V ₁ - V ₄ (Pins 2 & 3 Open) V _{CC} = 4.5 V, V _O = 2.4 V (Note 6) I _O ≤ 100 μA	2.87	3.70	4.20	V
I _{HYS}	Hysteresis		I _{HYS} = I _{TH+} - I _{TH-}	-	1.2		mA
V _{HYS}			V _{HYS} = V _{TH+} - V _{TH-}	-	1.3		V
V _{IHC1}	Input Clamp Voltage		V _{IHC1} = V ₂ - V ₃ , V ₃ = GND I _{IN} = 10 mA Pins 1 & 4 Connected to PIN 3	5.4	6.3	6.6	V
V _{IHC2}			V _{IHC2} = V ₁ - V ₄ , I _{IN} = 10 mA (Pins 2 & 3 Open)	6.1	7.0	7.3	V
V _{IHC3}			V _{IHC3} = V ₂ - V ₃ , V ₃ = GND I _{IN} = 15 mA (Pins 1 & 4 Open)	-	12.5	13.4	V
V _{IILC}			V _{IILC} = V ₂ - V ₃ , V ₃ = GND I _{IN} = -10 mA	-	-0.75	-	V
I _{IN}	Input Current		V _{IN} = V ₂ - V ₃ = 5.0 V (Pins 1 & 4 Open)	3.0	3.7	4.4	mA
V _{D1,2}	Bridge Diode Forward Voltage		I _{IN} = 3 mA	-	0.65		V
V _{D3,4}			I _{IN} = 3 mA	-	0.65		V
V _{OL}	Logic LOW Output Voltage		V _{CC} = 4.5 V, I _{OL} = 4.2 mA (Note 6)	-	0.04	0.4	V
I _{OH}	Logic HIGH Output Current		V _{OH} = V _{CC} = 18 V (Note 6)	-	-	100	μA
I _{CCL}	Logic LOW Supply Current		V ₂ - V ₃ = 5.0 V, V _O = Open V _{CC} = 5 V	-	1.0	4	mA
I _{CCH}	Logic HIGH Supply Current		V _{CC} = 18 V, V _O = Open	-	0.01	4	μA
C _{IN}	Input Capacitance		f = 1 mHz, V _{IN} = 0 V (Pins 2 & 3, Pins 1 & 4 Open)	-	50		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Logic LOW output level at pin 6 occurs when V_{IN} ≥ V_{TH+} and when V_{IN} > V_{TH-} once V_{IN} exceeds V_{TH+}.
Logic HIGH output level at pin 6 occurs when V_{IN} ≤ V_{TH-} and when V_{IN} < V_{TH+} once decreases below V_{TH-}.

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SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Propagation Delay Time (to Output Low Level)	$R_L = 4.7\text{ k}\Omega$, $C_L = 30\text{ pF}$ (Note 7)		6.0	15	μs
t_{PLH}	Propagation Delay Time (to Output High Level)	$R_L = 4.7\text{ k}\Omega$, $C_L = 30\text{ pF}$ (Note 7)		25.0	40	μs
t_R	Output Rise Time (10%–90%)	$R_L = 4.7\text{ k}\Omega$, $C_L = 30\text{ pF}$		45		μs
t_F	Output Fall Time (90%–10%)	$R_L = 4.7\text{ k}\Omega$, $C_L = 30\text{ pF}$		0.5		μs
ICM_{HI}	Common Mode Transient Immunity (at Output High Level)	$I_{IN} = 0\text{ mA}$, $R_L = 4.7\text{ k}\Omega$, $V_{Omin} = 2.0\text{ V}$, $V_{CM} = 1400\text{ V}$ (Notes 8, 9)		4000		$\text{V}/\mu\text{s}$
ICM_{LI}	Common Mode Transient Immunity (at Output Low Level)	$I_{IN} = 3.11\text{ mA}$, $R_L = 4.7\text{ k}\Omega$, $V_{Omax} = 0.8\text{ V}$, $V_{CM} = 1400\text{ V}$ (Notes 8, 9)		600		$\text{V}/\mu\text{s}$

ISOLATION CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{ISO}	Withstand Isolation Voltage	$RH \leq 50\%$, $I_{I-O} \leq 10\text{ }\mu\text{A}$, $t = 1\text{ min}$, $f = 50\text{ Hz}$ (Note 10, 11)	5,000	–	–	VAC_{RMS}
R_{I-O}	Resistance (Input to Output)	$V_{IO} = 500\text{ V}_{DC}$ (Note 10)	–	10^{12}	–	Ω
C_{I-O}	Capacitance (Input to Output)	$f = 1\text{ MHz}$, $V_{IO} = 0\text{ V}_{DC}$	–	0.6	–	pF

7. T_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 μs rise time) to the 1.5 V level on the leading edge of the output pulse. T_{PLH} propagation delay is measured on the trailing edges of the input and output pulse. (Refer to Fig. 10)
8. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0\text{ V}$). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8\text{ V}$). Refer to Fig. 11.
9. In applications where dV_{cm}/dt may exceed 50,000 $\text{V}/\mu\text{s}$ (Such as static discharge), a series resistor, R_{CC} , should be included to protect the detector chip from destructive surge currents. The recommended value for R_{CC} is 240 Ω per volt of allowable drop in V_{CC} (between pin 8 and V_{CC}) with a minimum value of 240 Ω .
10. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
11. The 5000 $\text{VAC}_{RMS}/1\text{ min.}$ capability is validated by a 6000 $\text{VAC}_{RMS}/1\text{ sec.}$ dielectric voltage withstand test.

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TYPICAL PERFORMANCE CURVES

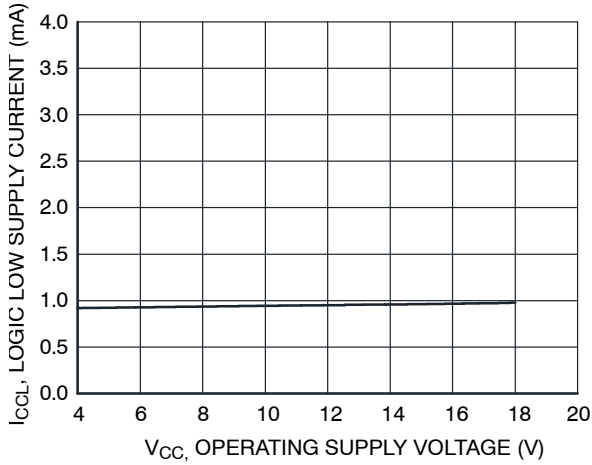


Figure 2. Logic Low Supply Current vs. Operating Supply Voltage

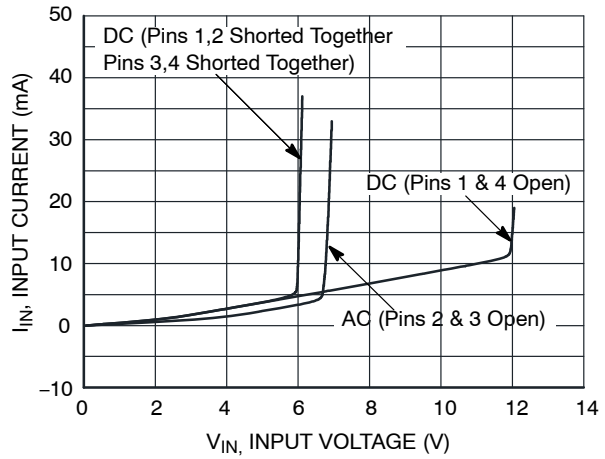


Figure 3. Input Current vs. Input Voltage

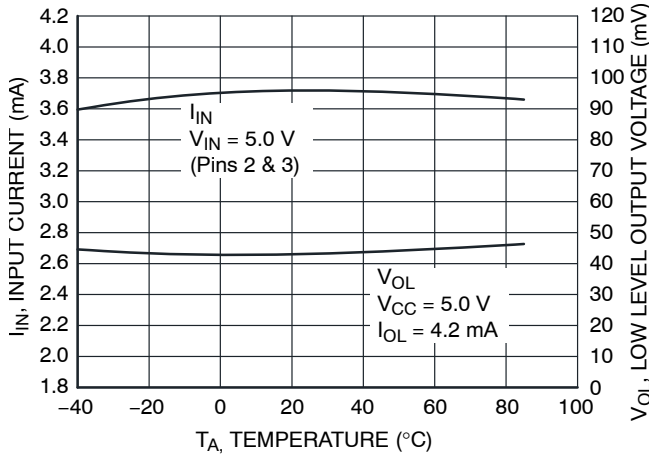


Figure 4. Input Current/Low Level Output Voltage vs. Temperature

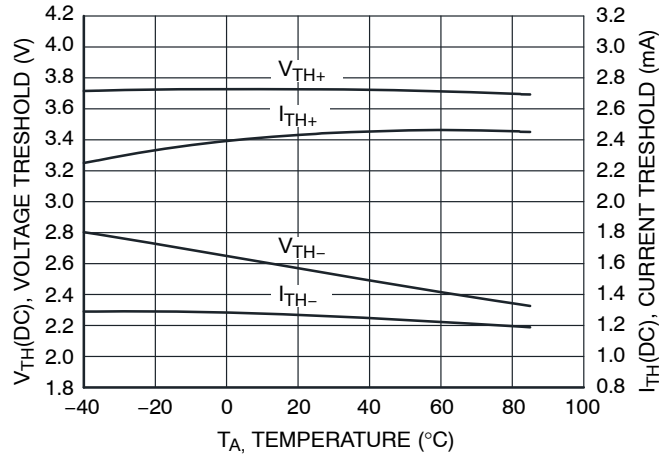


Figure 5. Current Threshold/Voltage Threshold vs. Temperature

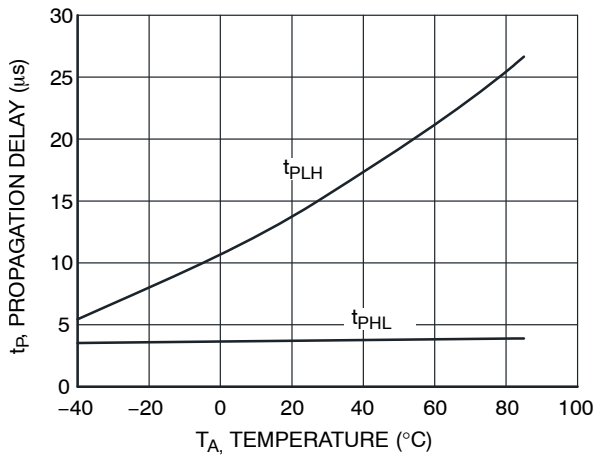


Figure 6. Propagation Delay vs. Temperature

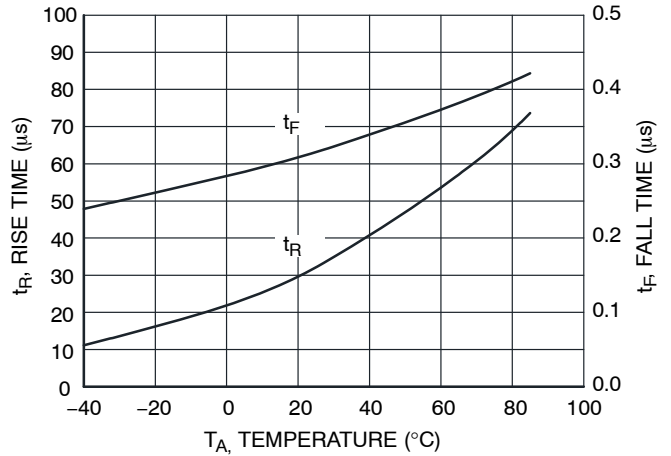


Figure 7. Rise and Fall Time vs. Temperature

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TYPICAL PERFORMANCE CURVES (continued)

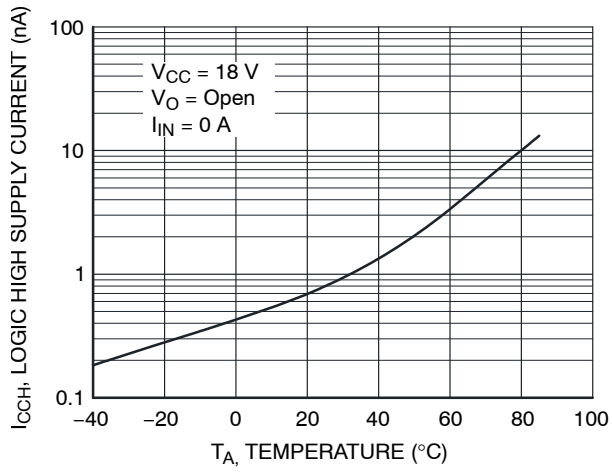


Figure 8. Logic High Supply Current vs. Temperature

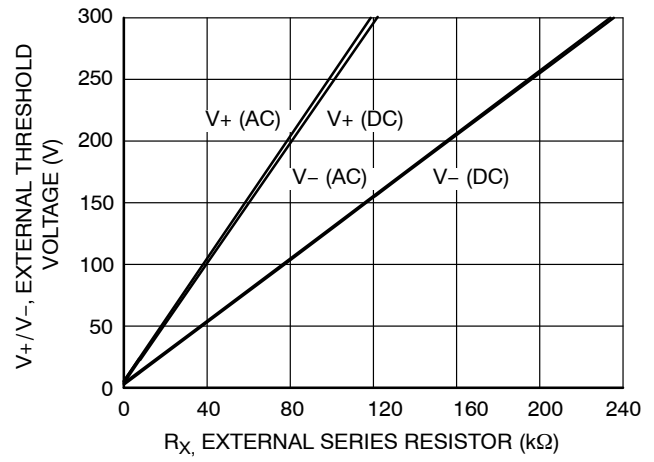
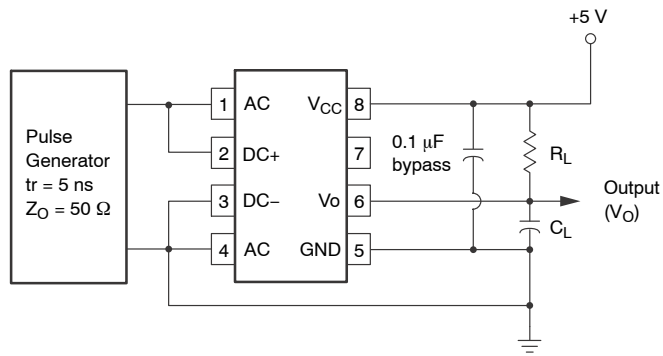


Figure 9. External Threshold Characteristics V_+/V_- vs. R_x

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TEST CIRCUITS



V_{IN}
 Pulse Amplitude = 50 V
 Pulse Width = 1 ms
 $f = 100 \text{ Hz}$
 $T_r = T_f = 1.0 \mu\text{s} (10\% - 90\%)$

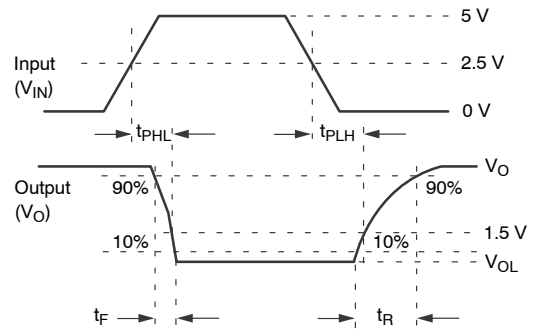
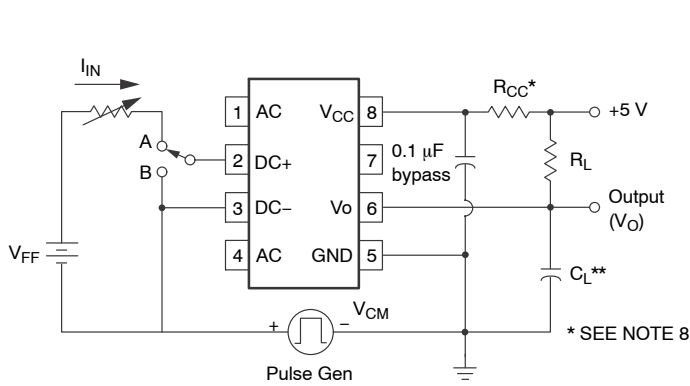


Figure 10. Switching Test Circuit



** C_L IS 30 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE

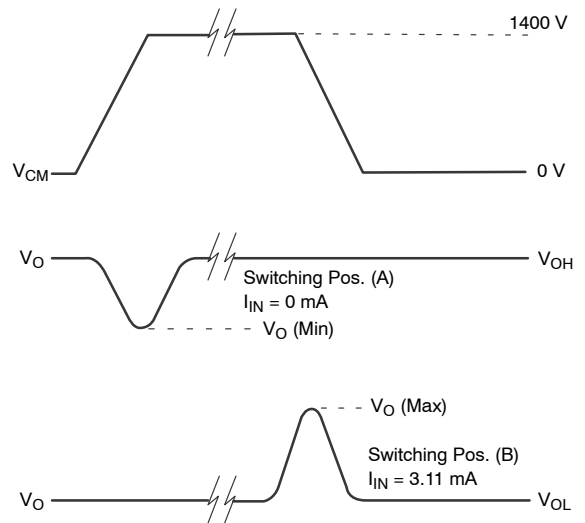
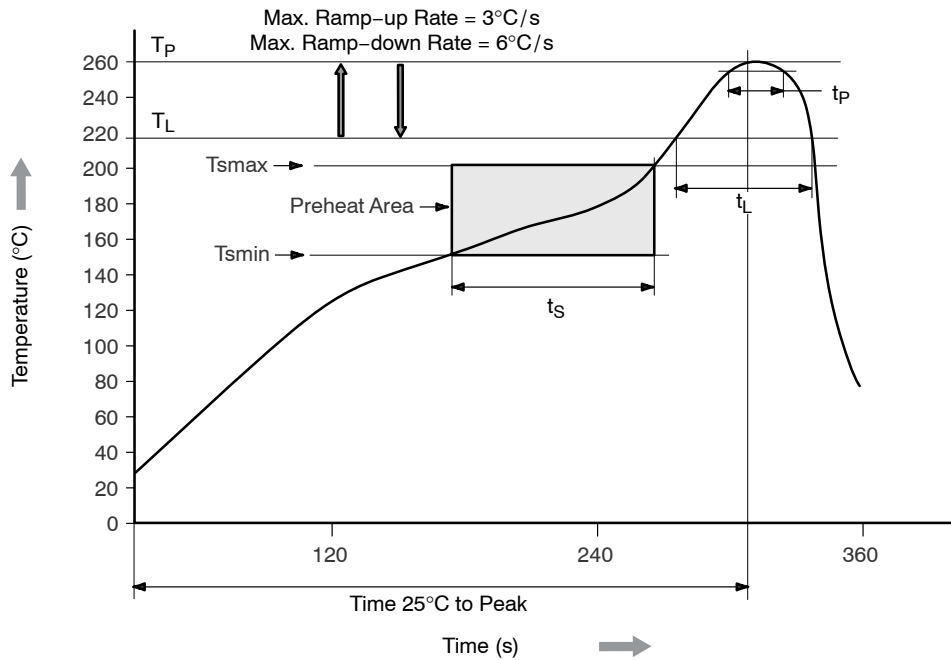


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

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REFLOW PROFILE



Profile Feature	Pb-Free Assembly Profile
Temperature Minimum (T _{min})	150°C
Temperature Maximum (T _{max})	200°C
Time (t _s) from (T _{min} to T _{max})	60 to 120 s
Ramp-up Rate (t _L to t _p)	3°C/s maximum
Liquidous Temperature (T _L)	217°C
Time (t _L) Maintained Above (T _L)	60 to 150 s
Peak Body Package Temperature	260°C +0°C/-5°C
Time (t _p) within 5°C of 260°C	30 s
Ramp-down Rate (T _P to T _L)	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

Figure 12. Reflow Profile

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ORDERING INFORMATION

Part Number	Package	Packing Method†
HCPL3700M	DIP 8-Pin	50 Units / Tube
HCPL3700SM	SMT 8-Pin (Lead Bend)	50 Units / Tube
HCPL3700SDM	SMT 8-Pin (Lead Bend)	1000 / Tape & Reel
HCPL3700VM	DIP 8-Pin, DIN EN/IEC60747-5-5 option	50 Units / Tube
HCPL3700SVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 option	50 Units / Tube
HCPL3700SDVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 option	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

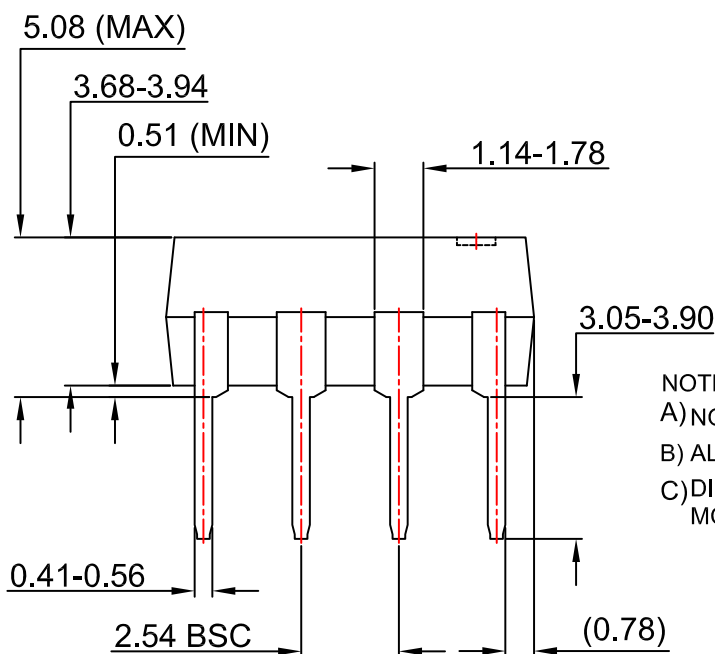
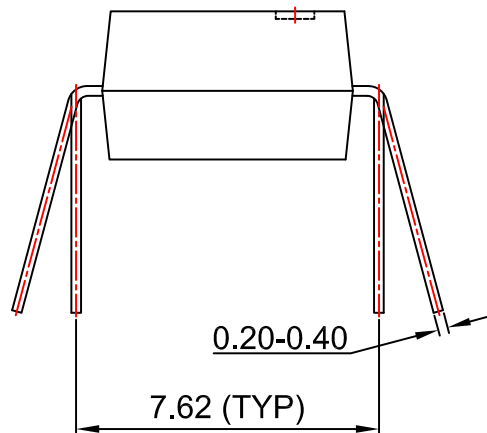
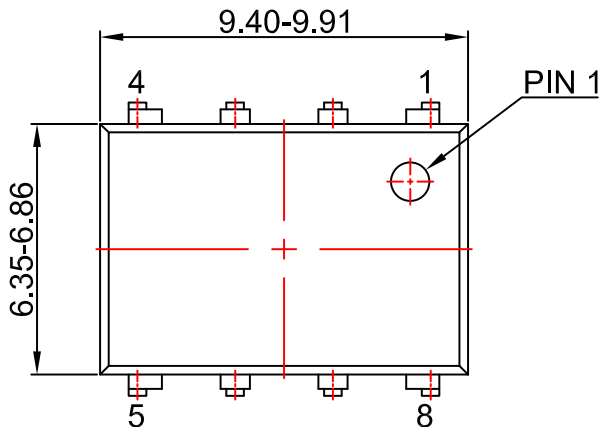
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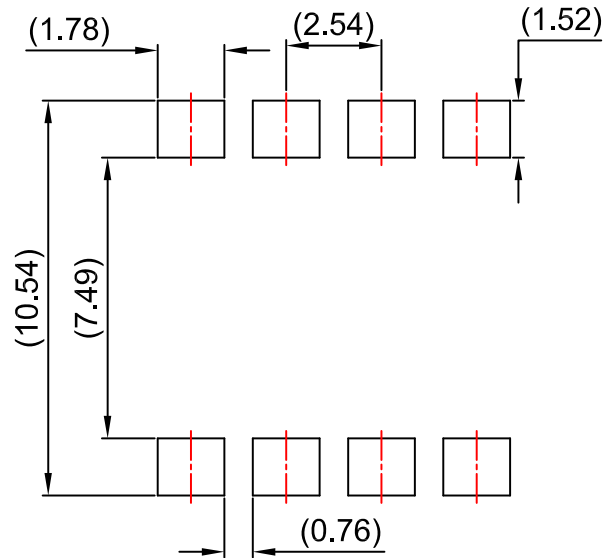
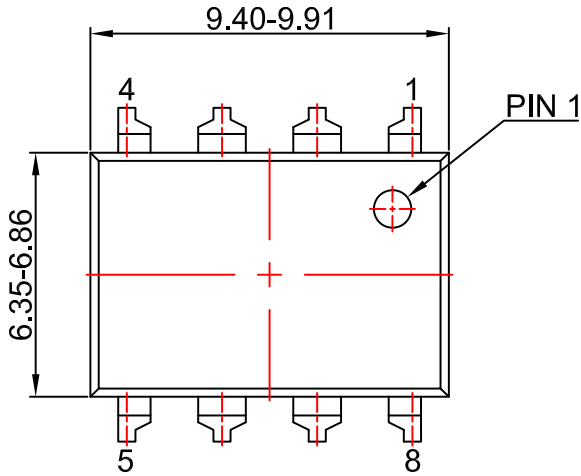
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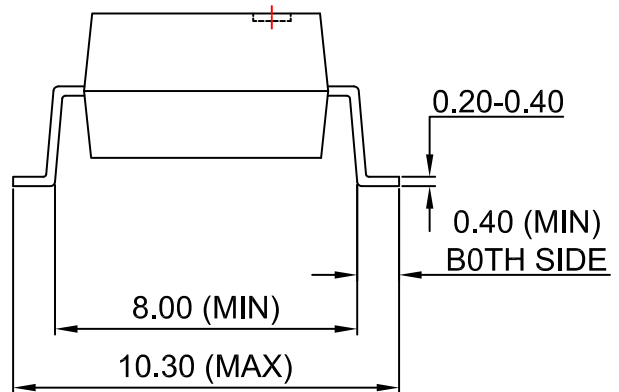
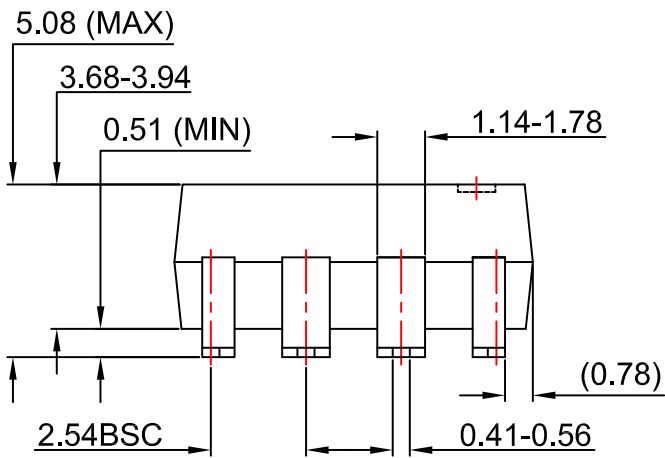


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ISSUE O

DATE 31 JUL 2016



LAND PATTERN RECOMMENDATION



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