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FAIRCHILD SEMICONDUCTOR®

July 2009

FMS6363 — Low-Cost, Three-Channel, 6th-Order, High-Definition, Video Filter Driver

Features

- Three Sixth-order 30MHz (HD) Filters
- Transparent Input Clamping
- Single Video Drive Load (2V_{pp}, 150Ω = 6δβ)
- AC or DC-coupled Inputs
- AC or DC-coupled Outputs
- DC-coupled Outputs Eliminate AC-coupling Capacitors
- 5V Only
- Robust 8kV ESD Protection
- Package SOIC-8

Applications

- Cable and Satellite Set-top Boxes
- DVD Players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

The FMS6363 low-cost video filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Three sixth-order filters provide improved image quality compared to typical lower-order passive solutions.

The FMS6363 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required *(see Applications section for details)*.

The outputs can drive AC-or DC-coupled single (150Ω) loads. DC-coupling the outputs removes the need for output coupling capacitors. The input DC levels are offset approximately +280mV at the output *(see Applications section for details)*.

Block Diagram

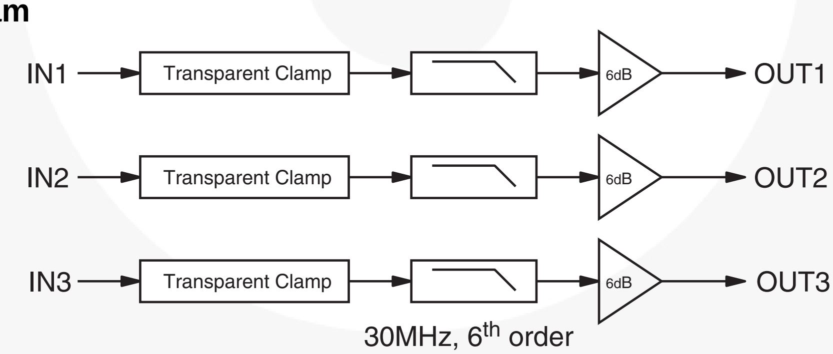


Figure 1. Block Diagram

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method	Quantity
FMS6363CS	0 to 70°C	RoHS	8-Lead, Small Outline Integrated Circuit (SOIC)	Rail	95
FMS6363CSX	0 to 70°C	RoHS	8-Lead, Small Outline Integrated Circuit (SOIC)	Reel	2500

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html

Pin Configuration

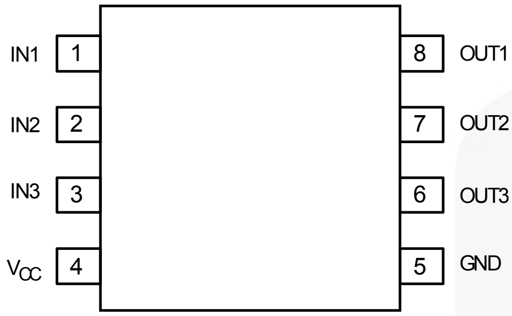


Figure 2. 8-Pin SOIC

Pin Definitions

Pin #	Name	Type	Description
1	IN1	Input	Video input, channel 1
2	IN2	Input	Video input, channel 2
3	IN3	Input	Video input, channel 3
4	V_{CC}	Input	+5V Supply
5	GND	Input	Ground
6	OUT3	Output	Filtered output, channel 3
7	OUT2	Output	Filtered output, channel 2
8	OUT1	Output	Filtered output, channel 1

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog Digital I/O	-0.3	V_{CC} + 0.3	V
I_{OUT}	Output Current, Any One Channel, Do Not Exceed		50	mA
ESD	Human Body Model, JESD22-A114		8	kV

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
T_L	Lead Temperature, Soldering 10 Seconds			+300	°C
θ_{JA}	Thermal Resistance, JEDEC Standard, Multi-layer Test Board, Still Air		112.7		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	0		70	°C
V_{CC}	Supply Voltage Range	4.75	5.00	5.25	V
R_{SOURCE}	Input Source Resistance			300	Ω

DC Electrical Characteristics

T_A=25°C, V_{CC}=5V, R_{SOURCE}=37.5Ω, inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply Current(1)	No Load		22	30	mA
V_{IN}	Video Input Voltage Range	Referenced to GND, if DC-coupled		1.4		V_{PP}

Note:
1. 100% tested at 25°C.

AC Electrical Characteristics

T_A=25°C, V_{IN}=1V_{PP}, V_{CC}=5V, R_{SOURCE}=37.5Ω, inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into150Ω loads, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV	Channel Gain(2)	All Channels	5.8	6.0	6.2	dB
f_{1dB}	-1dB Bandwidth(2)	All Channels	23	30		MHz
f_C	-3dB Bandwidth	All Channels	30	33		MHz
f_{SB1}	Attenuation, Stopband Reject	All Channels at f=37.125MHz		6.5		dB
f_{SB2}		All Channels at f=44.25MHz		14.5		
f_{SB3}		All Channels at f=74.25MHz(2)	32	36		
THD1	Output Distortion, All Channels(3)	V_{OUT}=1.4V_{PP}, 10MHz		0.2		%
THD2		V_{OUT}=1.4V_{PP}, 15MHz		0.4		
THD3		V_{OUT}=1.4V_{PP}, 22MHz		1.2		
X_{TALK}	Crosstalk Channel-to-Channel	At 1MHz		-60		dB
SNR1 SNR2	Signal-to-Noise Ratio, All Channels(4)	Unweighed; 30MHz lowpass, 100KHz to 30HKz		65		dB
t_{pd}	Propagation Delay	Delay from input to output		20		ns

Notes:
2. 100% tested at 25°C.
3. 1.4V_{PP} active video.
4. SNR=20 • log (714mV/rms noise).

Typical Performance Characteristics

T_A=25°C, V_{CC}=5V, R_{SOURCE}=37.5Ω, inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into150Ω loads, referenced to 400kHz; unless otherwise noted.

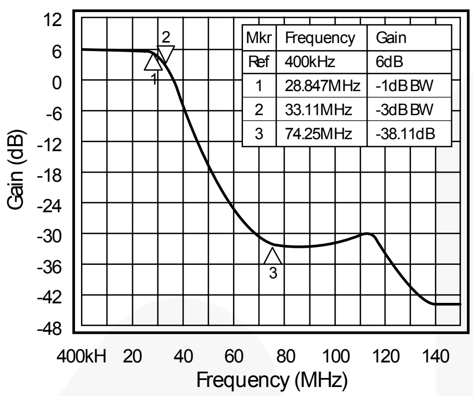


Figure 3. Frequency Response

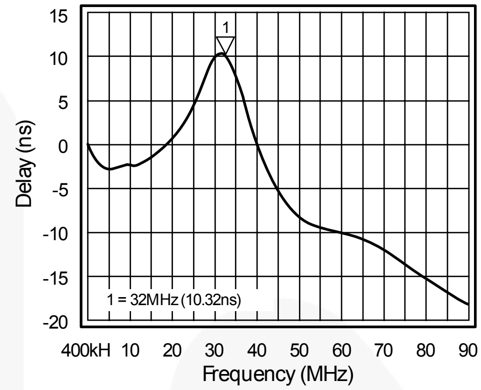


Figure 4. Group Delay vs. Frequency

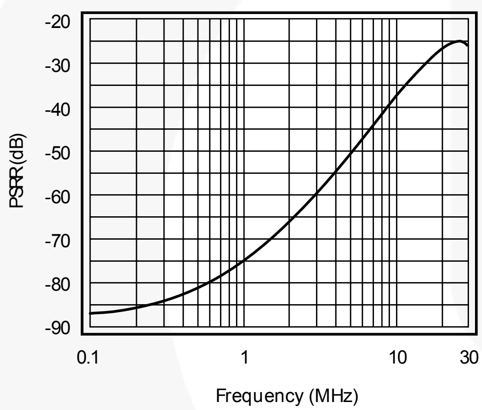


Figure 5. PSRR vs. Frequency; No Bypass Caps

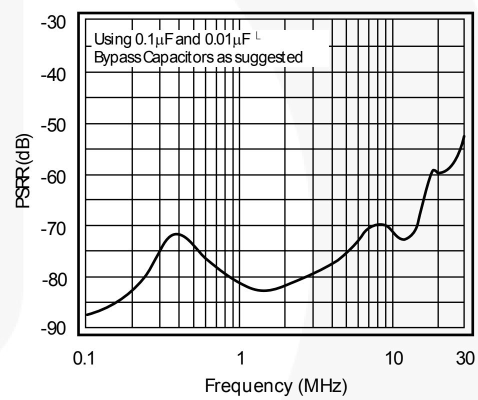


Figure 6. PSRR vs. Frequency; Bypass Caps

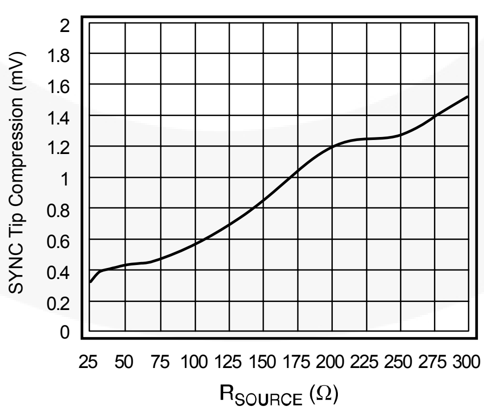


Figure 7. SYNC Tip Compression vs. R_{SOURCE}

Applications Information

Functional Description

The FMS6363 Low-Cost Video Filter (LCVF) provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in Figure 8.

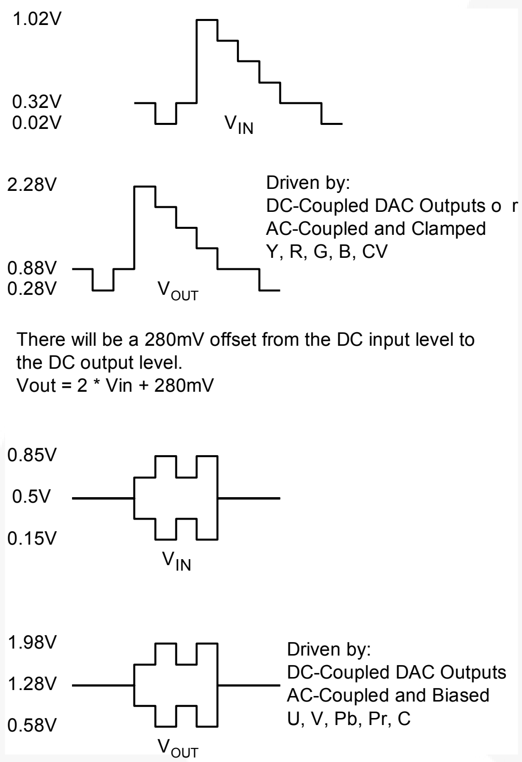


Figure 8. Typical Voltage Levels

The FMS6363 provides an internal diode clamp to support AC coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the FMS6363 without an AC coupling capacitor. The worst-case sync tip compression due to the clamp does not exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range. When the input is AC-coupled, the diode clamp sets the sync tip (or lowest voltage) just below ground.

For symmetric signals like C, U, V, Cb, Cr, Pb and Pr; the average DC bias is fairly constant and the inputs can be AC-coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 9.

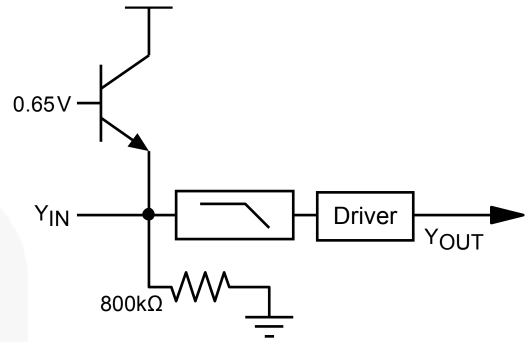


Figure 9. Input Clamp Circuit

I/O Configurations

For DC-coupled DAC drive with DC-coupled outputs, use the configuration in Figure 10.

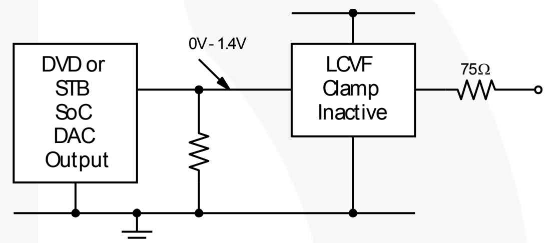


Figure 10. DC-coupled Inputs and Outputs

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC-coupled, as shown in Figure 11.

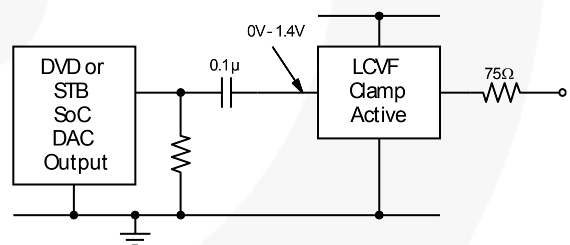


Figure 11. AC-coupled Inputs, DC-coupled Outputs

When the FMS6363 is driven by an unknown external source or a SCART with its own clamping circuitry the inputs should be AC-coupled, shown in Figure 12.

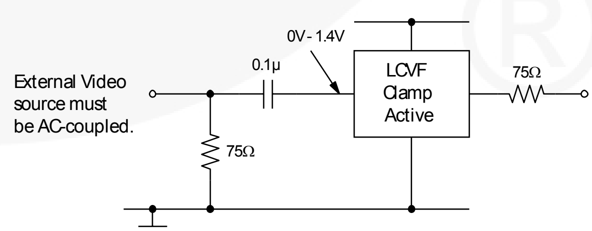


Figure 12. SCART with DC-coupled Outputs

The same method can be used for biased signals with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is 800kΩ ±20%, so the external resistance should be 7.5MΩ to set the DC level to 500mV. If a pull-up resistance of less than 7.5MΩ desired, add an external pull-down such that the DC input level is set to 500mV.

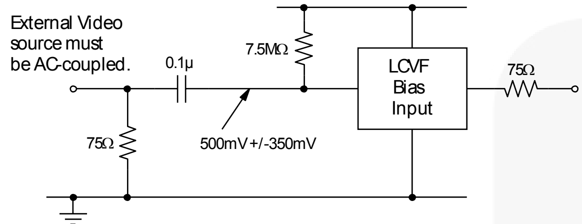


Figure 13. Biased SCART with DC-coupled Outputs

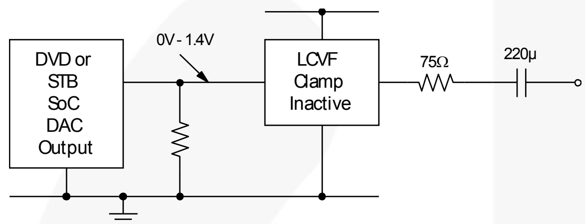


Figure 14. DC-coupled Inputs, AC-coupled Outputs

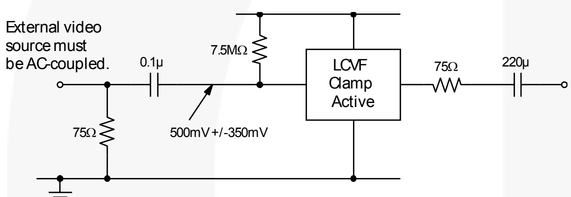


Figure 15. Biased SCART with AC-Coupled Outputs

Note: The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220µF to obtain satisfactory operation in some applications.

Power Dissipation

The FMS6363 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the FMS6363's power dissipation and internal temperature rise.

$T_J = T_A + P_d \bullet \Theta_{JA}$ (1)

where $P_d = P_{CH1} + P_{CH2} + P_{CH3}$

and $P_{CHx} = V_S \bullet I_{CH} - (V_{O2}/R_L)$

where

$V_O = 2V_{IN} + 0.280V$

$I_{CH} = (I_{CC}/3) + (V_O/R_L)$

V_{IN} = RMS value of input signal

$I_{CC} = 24mA$

$V_S = 5V$

R_L = channel load resistance

Board layout affects thermal characteristics. *Refer to the Layout Considerations section for more information*.

The FMS6363 is specified to operate with output currents typically less than 50mA, more than sufficient for a single (150Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief duration, short-circuit conditions; however, this capability is not guaranteed.

Output Considerations

The FMS6363 outputs will be DC offset from the input by 150mv therefore $V_{OUT} = 2*V_{IN}$ DC+150mv. This offset is required to obtain optimal performance from the output driver and is held at the minimum value in order to decrease the standing DC current into the load. Since the FMS6363 has a 2x (6dB) gain, the output is typically connected via a 75Ω series back-matching resistor followed by the 75Ω video cable. Because of the inherent divide by two of this configuration, the blanking level at the load of the video signal is always less then 1V. When AC-coupling the output ensure that the coupling capacitor of choice will pass the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input being driven. In order to obtain the highest quality output video signal the series termination resistor must be placed as close to the device output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the FMS6646 output driver. Recommend distance from device pin to place series termination resistor should be no greater than 0.1 inches.

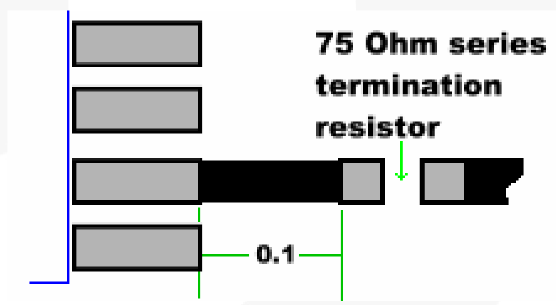


Figure 16. Distance from Device Pin to Series Termination Resistor

Layout Considerations

Layout and supply bypassing play major roles in high-frequency performance and thermal characteristics.

For optimum results, follow the steps below as a basis for high-frequency layout:

- Include 10μF and 0.1μF ceramic bypass capacitors
- Place the 10μF capacitor within 0.75 inches of the power pin.
- Place the 0.1μF capacitor within 0.1 inches of the power pin.
- Connect all external ground pins as tightly as possible, preferably with a large ground plane under the package.
- Layout channel connections to reduce mutual trace inductance.
- Minimize all trace lengths to reduce series inductances. If routing across a board, place device such that longer traces are at the inputs rather than the outputs. If using multiple, low-impedance DC-coupled outputs, special layout techniques may be employed to help dissipate heat.

If a multilayer board is used, a large ground plane directly under the device helps reduce package case temperature.

For dual-layer boards, an extended plane can be used.

Worst-case additional die power due to DC loading can be estimated at ($V_{CC}^2/4R_{load}$) per output channel. This assumes a constant DC output voltage of V_{CC}^2. For 5V V_{CC} with a dual DC video load, add 25/(4•75) = 83mW, per channel.

Typical Application

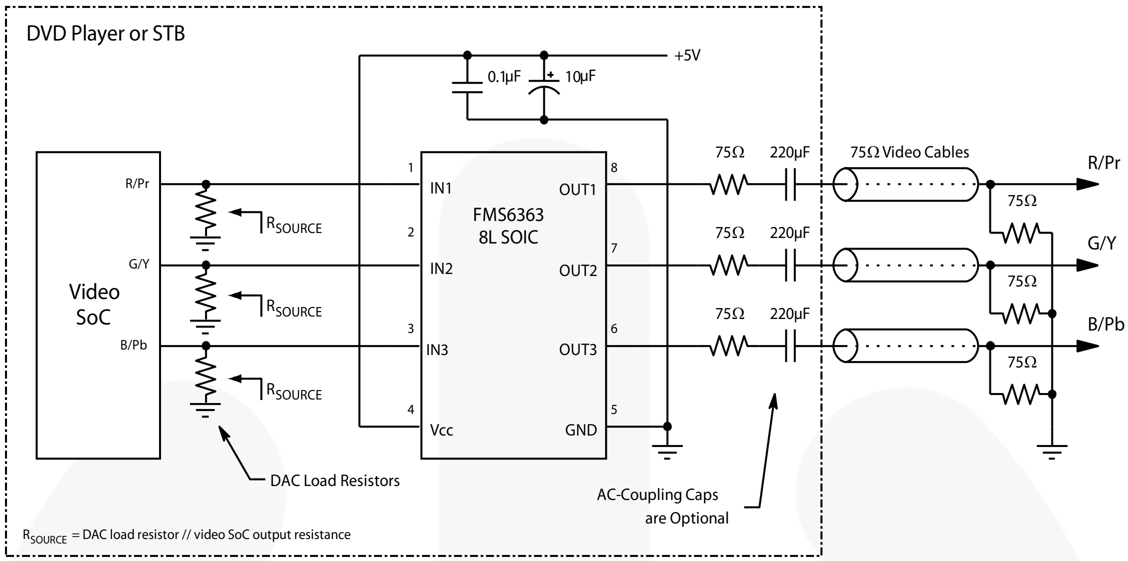
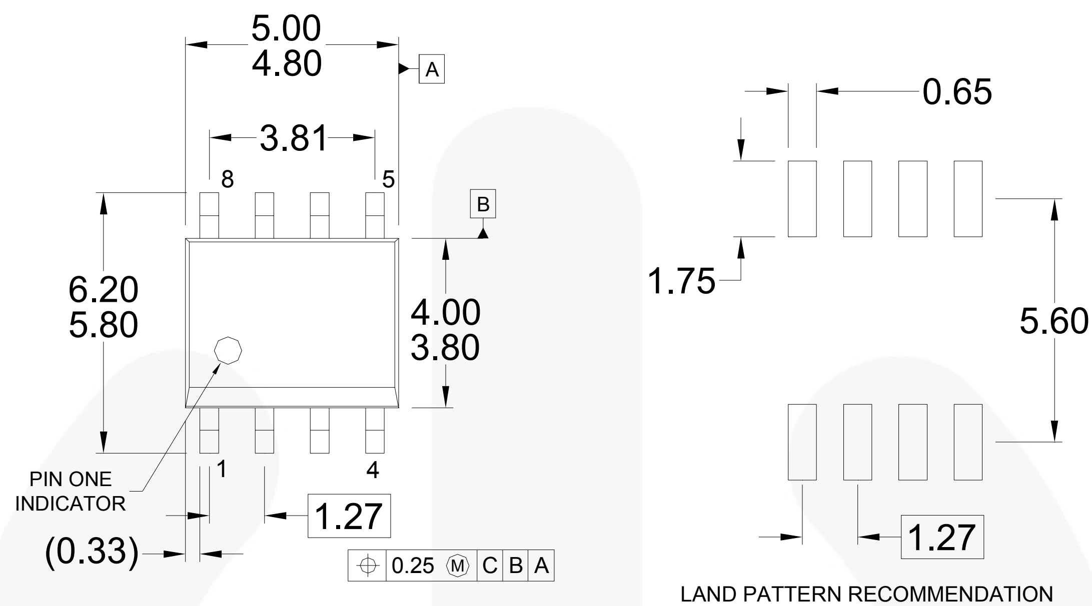
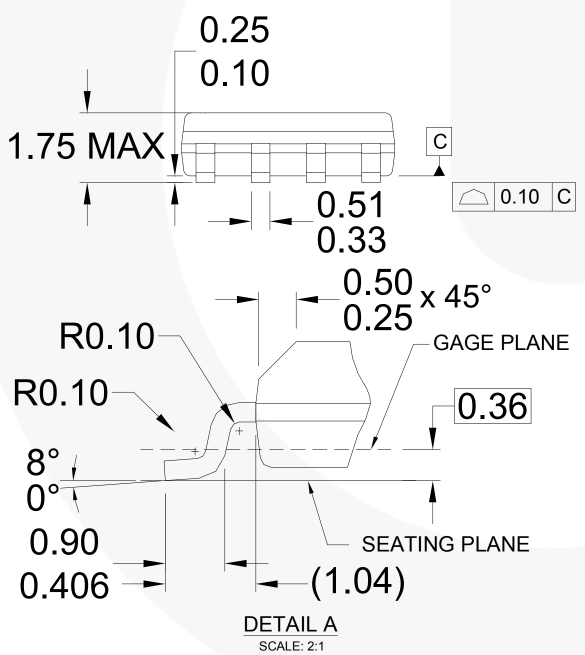


Figure 17. Typical Application Diagram

Physical Dimensions





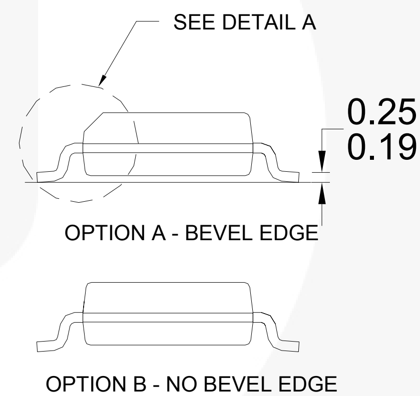


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Figure 18. 8-Lead, Small Outline Integrated Circuit (SOIC) Package

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I42

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