On Board Charger (OBC) Three-phase PFC Converter

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Summary

With the coming electrification of the automotive market, the need of battery chargers is more and more demanded. With the simple equation more power, shorter the recharge time is, a 3−phase supply is here considered which can provide up to '3x' the power of a single−phase supply.

The 3−phase PFC board here proposed is an example of the first stage of an On Board Charger system based on silicon carbide MOSFET which will lead to a higher system efficiency and a reduced BOM content.

The board is developed with the primarily goal of providing easy access to the different devices for easing the testing phase and for measuring; a form factor optimization has never been a target for the EVB.

Output Voltage

The output voltage provided by the 3−phase PFC is here fixed to 700 V (Accuracy 5%) and thanks to the SiC technology, the thermal capability can be extended to higher ranges. The max deliverable power is 11 kW considering an input voltage of 230 Vac at 50 Hz.

System

- High f_s Range (60−140 kHz)
- High Efficiency (98.3% @ f_s 100 kHz)
- Wide Input Range (167 to 265 V_{PH} rms)
- Bi−Directional
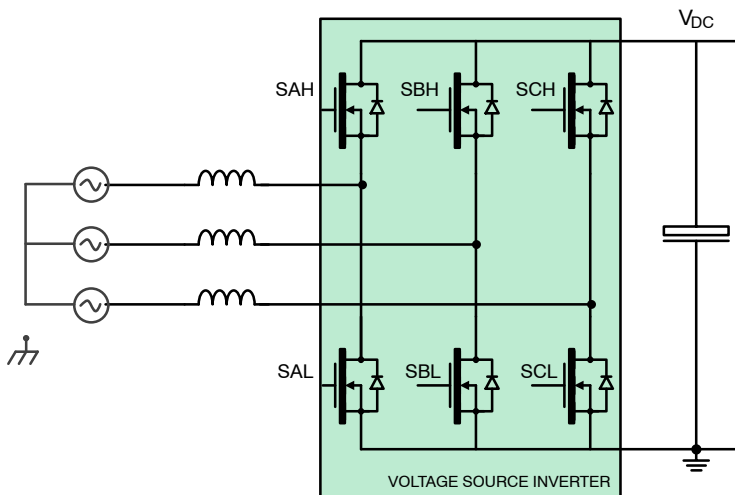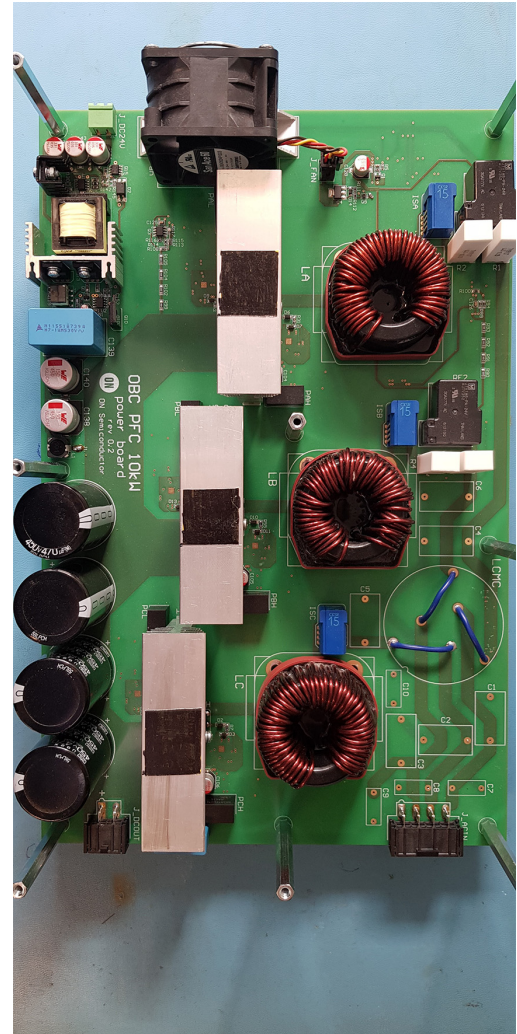- 3 Phase Full Bridge Rectifier

Figure 1. Board Photo
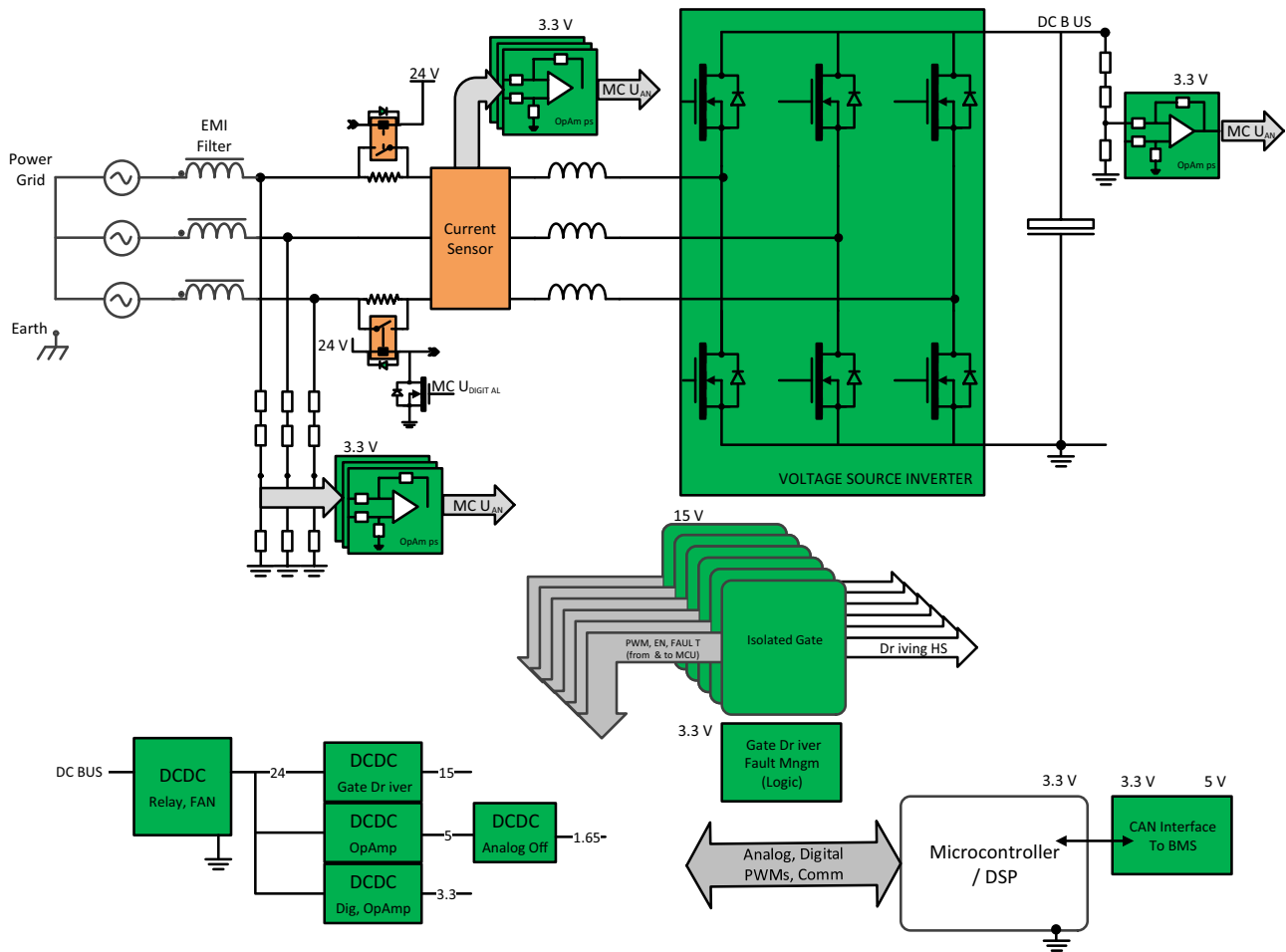

Figure 2. Topology – High Level

Figure 3. 3−Phase PFC Block Diagram

APPLICATION/CONTROL OVERVIEW

Overall concept can be seen in Figure 3. Since testability was set as the highest priority during concept definition, the board presented does not aim for highest power densities and/or compactness.

The board behavior is simple, when a 3−phase voltage at 50 Hz is provided to the input connector; the output bus capacitor voltage will rise because of nature of the PFC topology. A bridge−less PFC with MOSFET guarantees a current path from input to output because of the parasitic freewheeling diode present on each MOSFET. When the MOSFET are all off, the board simplifies in a 3−phase diode bridge. The rectified input AC voltage will set to a defined level depending on the supply voltage amplitude and on the forward voltage of the MOSFET body diodes, however it is expected that at least 167 Vrms are given at the input. For this reason, a resistor on two different lines serves as inrush current limiter. Once the bus voltage reaches 400 V, the 2−switch flyback converter starts to operate. It provides 24 V from which a series of DC/DC regulators generate the other needed voltage levels for powering up the digital and analog circuitry.

When the micro awakes, besides verifying the offset voltages for the ADC channels, it starts also monitoring the bus voltage and sensing the input voltages from which determines the frequency and the angle of the phase voltages. Such angle will be the reference angle of the system to achieve the power factor correction.

When the DC bus voltage becomes flat, the MCU issues a command to the relay to bypass the resistor and allow a further boost in the output bus voltage. However, the voltage increment is going to be something lower the rectified input voltage amplitude, $\sqrt{6} \cdot V_{PH, RMS}$.

MCU will wait until the bus voltage becomes flat again in order to start controlling the bus voltage to the targeted value of 700 V. Target value does not change in a single step but a smooth ramp generator will bring the bus value according a parametrized slope to the final 700 V.

The PFC implements only one hardware protection, against overcurrent events leveraging the DESAT functionality of the NCV51705 gate driver. A threshold value of 50 A is set on the board given the characteristic of the NVHL080N120SC1 Silicon Carbide MOSFET (N−Channel, 1200 V, 80 mΩ, TO247−3L).

All the fault lines are collected together to generate a single input to the MCU which provides a hardware stop to the PWM generation. A reset of the failure conditions is possible only by a reset command sent through a GUI or by a power down/power up sequence, basically it represents a HW/SW reset. The Figure 4 summarizes the high level SW behavior.
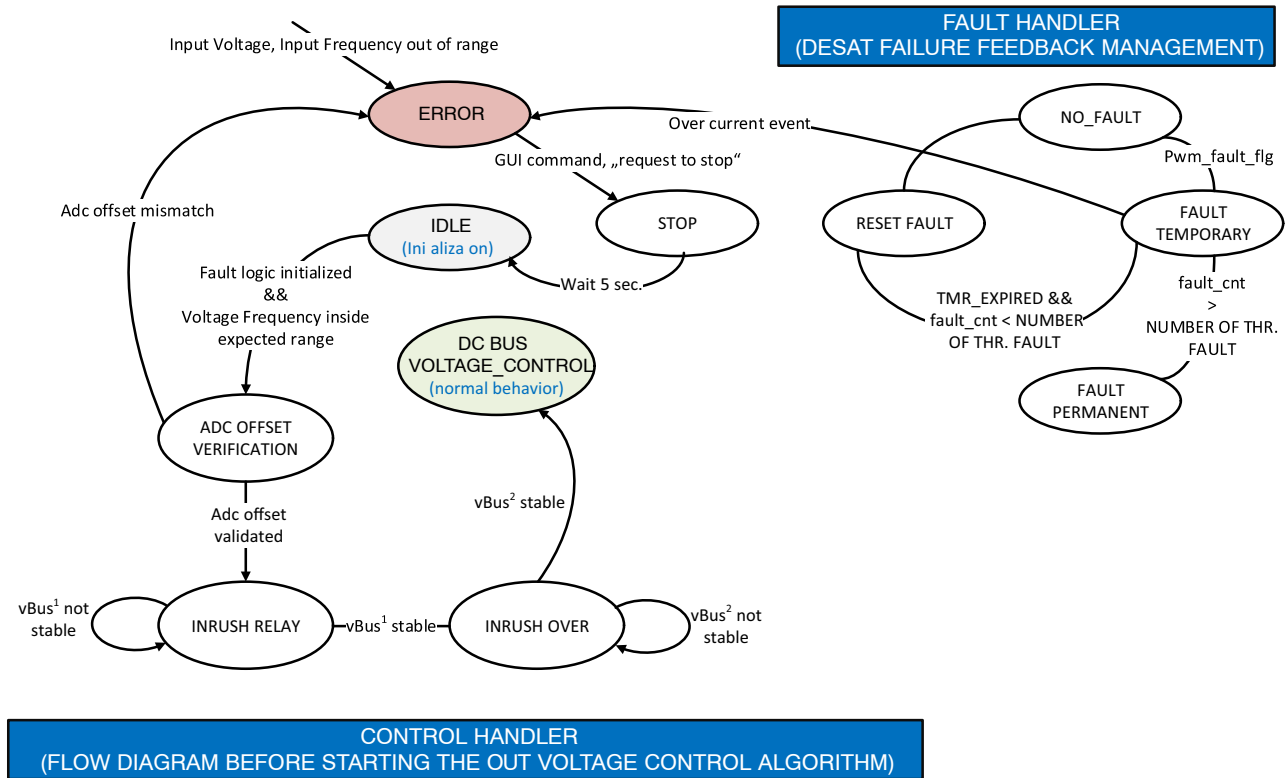

Figure 4. Flow Diagram of Preliminary Steps before Activating DC Bus Voltage Regulation

Once the application is sitting in the DC BUS voltage control state and in case of no failure events, the MCU will run the field oriented (FOC) voltage control algorithm.

The control algorithm is similar to a motor control one where the inner loops control the current components. Outer loop controls the bus voltage. Since the goal of the PFC is to guarantee 0° of phase delay between each phase voltage and phase current, the voltage regulation acts on the D−axes current. Q−axes current is set to be 0. D−axes represents the "ACTIVE" power branch, while Q−axes represents the "REACTIVE" power branch. Figure 5 shows the block diagram of the control algorithm.
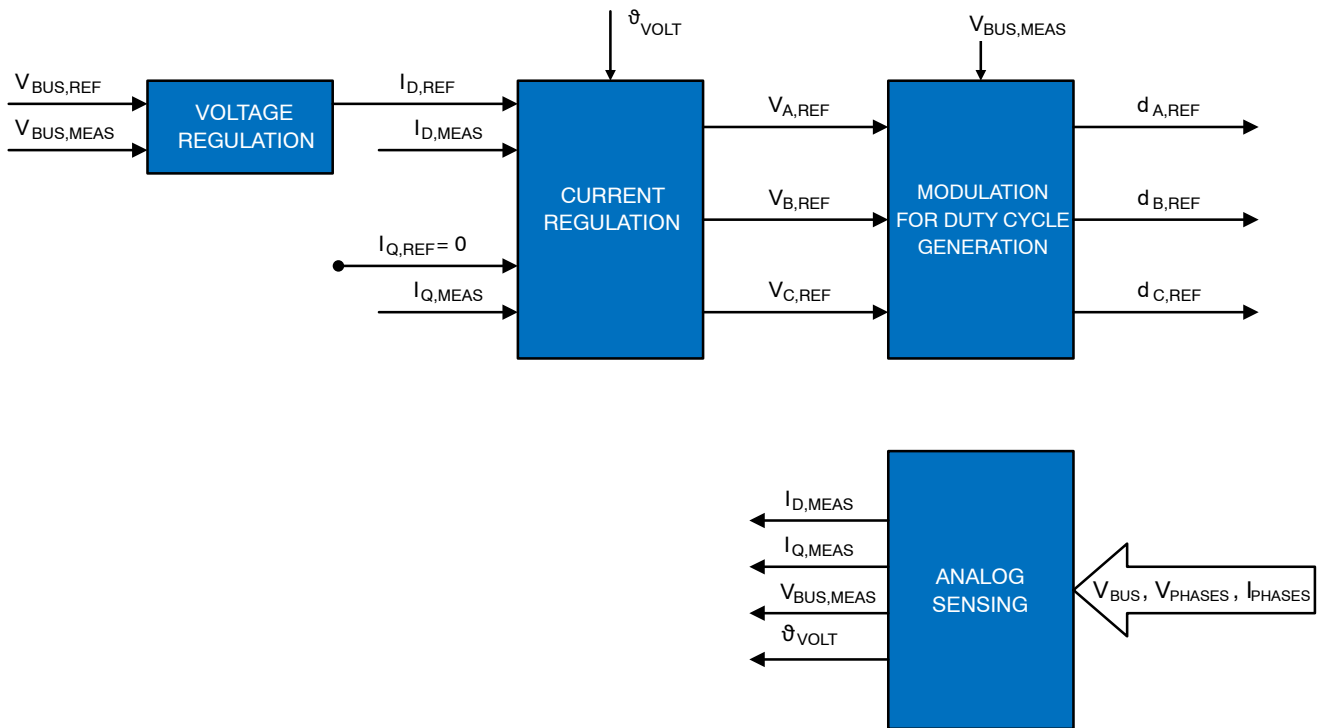
Figure 5. Control Block Diagram

The analog quantities sampled to perform the control algorithm are:
- Phase currents (x3);
- Line voltages, since the neutral point is not provided at the input connector (x3);
- DC bus voltage.

The line to line voltages are used to determine the actual position of the AC voltage phasor. The angle, theta, is then used for regulated the current phase delay to 0° that is the main target of the PFC. The voltage position is used for switching from stationary ABC system reference into the rotating DQ frame by means of Clark and Parke transformation (for the PFC, D axes means the amplitude of the phase voltage phasor).

By knowing theta, all the electrical quantities can be then expressed in the DQ system, such simplification will ensure the usage of simple PI/PID regulators. Just as a side note, PID stands for Proportional Integral and Derivative regulation that may be applied singularly or a combination of them to the system. In any case, the proper selection depends on the transfer function of the plant to be regulated.

PI regulators indeed can effectively regulates an error to zero when a constant is provided as reference quantity, while are not capable of regulating AC reference quantities. In any case, a calibration of PI regulators are needed in order to ensure proper system stability with a good trade−off between PI loop bandwidth and time response. It is typical to expect fast response for the current loop (internal) and lower response on the external loop (voltage).

In the Figure 7, a more detailed picture of the implemented control loop is provided. Such control loop is running at 20 kHz no matter what is going to be the selected PWM modulation frequency. PWM frequency is almost independent from the control frequency although there is a synchronization procedure in place in order to have ADC peripheral triggered by a specific PWM counter value.

This procedure allows to keep a good relationship among phase currents, in a star connected three−phase system with isolated neutral it is expected to have the instantaneous value of the sum of the current equal to zero.

The MCU selected is a general−purpose one, based on an Arm® M3, clock frequency 84 MHz, single S/H and ADC with multiplexed input channels, 1 MSPS, and 12 bits. Delay time for one ADC conversion is around 1 μs.

Because of the reading delay, of the fast PWM frequency, of the instantaneous switches' status and of the boost inductance, the current flowing in each phase can change quite significantly in very short time. Therefore, in order to overcome such problematic situation, the currents are sampled across three continuous PWM periods. This means that the minimum PWM frequency selectable for a proper functionality is three times the control strategy, thus 60 kHz. Limitations of course are also present on the max PWM frequency allowed, and it is 140 kHz. This limitation is introduced by the wait time needed to perform the measurement in each PWM period before triggering again the ADC peripheral for a new measurement. Figure 6 displays the reason behind this limitation.
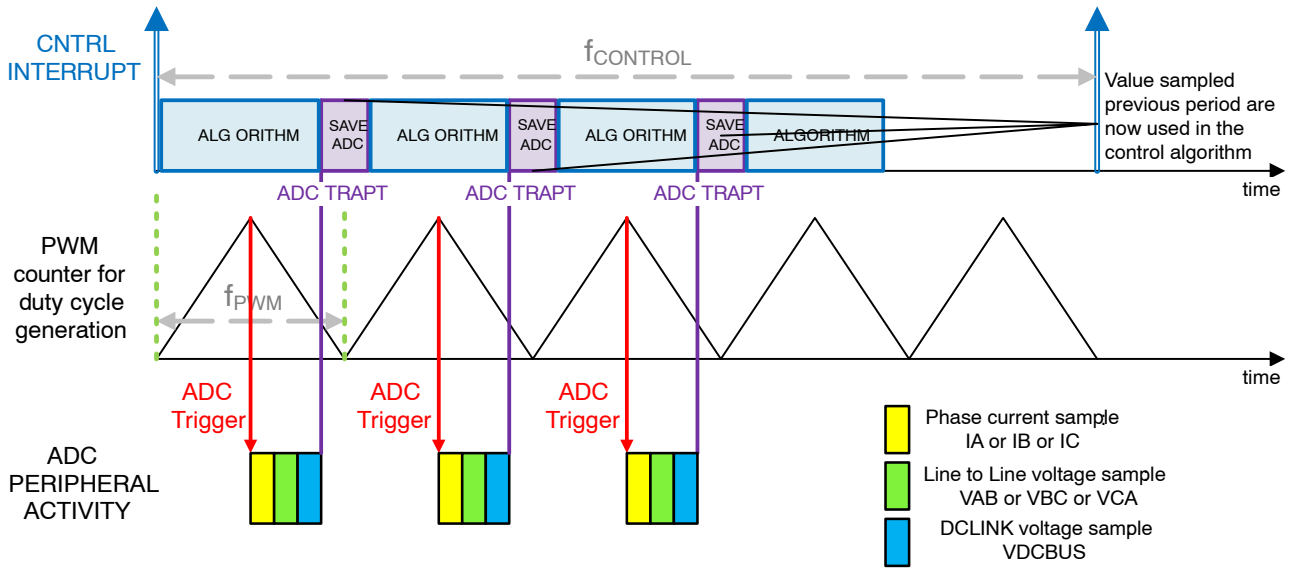
Figure 6. Main Peripheral Interaction and Control Algorithm Execution

As can be seen from Figure 6, a new ADC trigger can be issued only once the three analog quantities (1 current and 2 voltages) have been sampled and the end of conversion interrupt from the ADC has been issued to the CPU to store the result data registers into memory and prepare the ADC for a new measurement. Each procedure requires around 3.5 μs. After three PWM periods, ADC is no longer triggered until a new control interrupt is happening that re−initialize the reading strategy.

The quantities collected during a control period will be used at the next available control period. There is a deterministic delay between the moment when the analog quantities is sampled from the ADC and the moment when it is effectively used in the control strategy. Such delay, however, is not compensated; the reason is because the main working frequency is well below the selected control frequency period and therefore the delay is treated as negligible.

Once available the ADC quantities, the control implementation is straightforward, Figure 7.
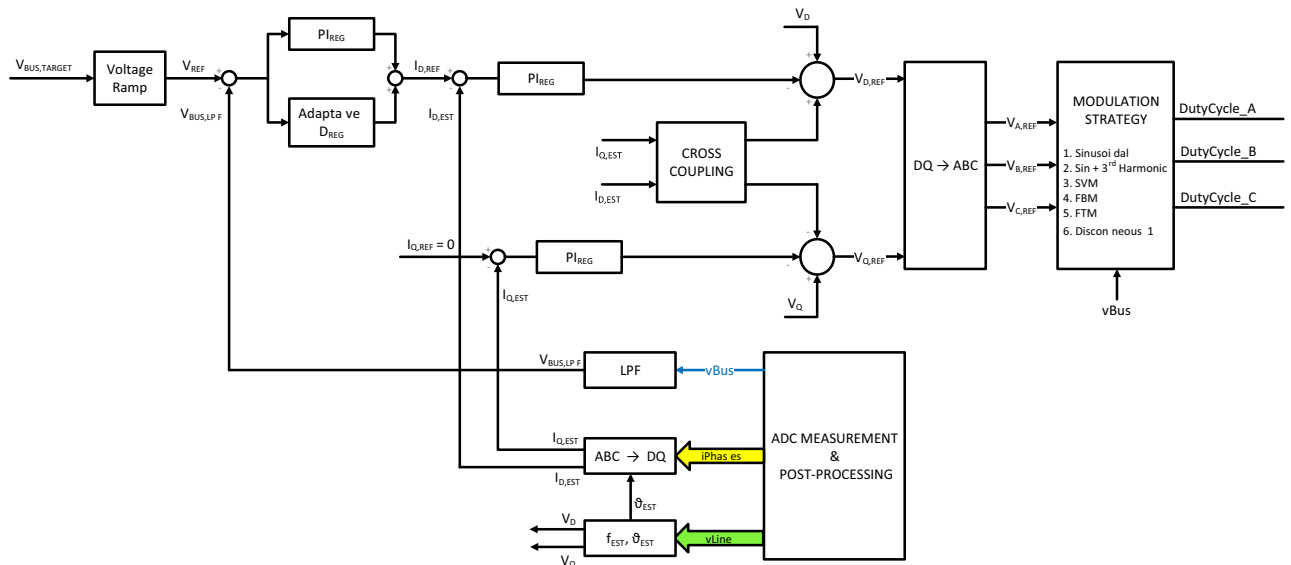
Figure 7. Control Algorithm, Detailed Description

As said earlier, the modulation frequency can be selectable in a range between 60 kHz to 140 kHz and this is what it is the benefit of using silicon carbide MOSFET. Of course, from system behavior point of view, increasing the switching frequency will imply higher switching losses, which will heat up substantially the die and will increase, in turn, the conduction losses since $R_{DS,ON}$ increases with the temperature. For this reason it has been foreseen on the board a fan with the intent of keeping the heatsink on which the SiC MOSFETs are mounted, cooled down. The fan is driven by the MCU but, at the moment, its speed is kept fixed. A fan speed regulation could be implemented according the active power delivery which is direct proportional to $I_{D,REF}$.

In order to mitigate losses and improve system efficiency, different driving strategies can be implemented. Some more details are provided in the results section.

HW OVERVIEW

The system consists of two boards: a 4−layer power board and a 4−layer control board.

The power board embeds:
- All the circuit from the input to the bus voltage (relays, boost inductors, SiC MOSFETs, dc bus cap),
- First level circuitry for analog signal conditioning (treated into 5 V range),
- A fan and its driving circuitry,
- Gate driver sub−systems (replicated for each MOSFET),
- High to 24 V DCDC converter,
- Distributed connectors to minimize the loops length at the switching nodes.

The control board embeds:
- The microcontroller and the circuit for his isolated programming (through serial communication),
- 24 to various DC voltage level as depicted in Figure 3.
- Second level analog signal conditioning, taking the power boards inputs and adjusting to 3.3 V range.
- Logic gates to handle the fault signals coming from the gate drivers.
- LEDs and distributed connectors as per power board.

FAN

The fan requires two pins:
- FAN_ON_OFF: setting the pin high will provide the 24 V to the fan.
- FAN_PWM: this is a pulse width modulated pin. Higher duty will result in an increasing fan speed, thus an increased forced air.

RELAYS

The relays layout foresees that at power on, the 13.6 Ω power resistors mounted on the board are limiting the inrush current. Resistor is disconnected by toggling the INRUSH_OFF pin setting the digital value to high. At power up, such pin is initialized low.

Gate Driver System

The board is provided with six symmetric structures of gate drivers. Each of them consists of an isolated DCDC converter, a digital isolator and the NCP51705 gate driver. NVP51705 is a dedicated device for driving SiC MOSFET. Each section presents 3 digital pins: 2 inputs and 1 output (from gate driver prospective; 2 outputs and 1 input if considering from MCU side). MCU has to provide for each driver a disable signal; it actually represents the negated input of the PWM signal, and the PWM signal itself. MCU has to sense the fault pin. It represents a failure condition at gate driver level.

In order to understand better the gate driver operation, refer to the gate driver datasheet available at onsemi.com website.

When a gate driver failure is established, the gate driver will automatically disable the PWM output. The fault pin is used for signaling to the MCU a failure condition. Such failure is normally introduced because of an over current event, although it could be also triggered by additional abnormal conditions.

Once a failure event is happening, the PWM signals are no longer provided to the gate drivers and the disable pin is again engaged.

The fault pin of each gate driver is collected in an "or" port with six inputs. The resulting PWM_FAULT is then connected to the hardware PWM failure pin available on the MCU.

DISABLE pin should be initialized as HIGH in order to disable the gate driver functionality. When the control strategy is capable of sending valid duty cycle information, DISABLE has to be set low.

TESTING

The following test results are generated supplying the board with 230 Vrms at 50 Hz.

The control algorithm is configured to provide a switching frequency of 100 kHz with 100 ns of dead−time. The boost inductor used has an average inductance value of 330 μH.

The gate resistor values for driving the MOSFET are 22 Ω for sourcing and 4.7 Ω for sinking ensuring the following switching characteristic at maximum current:
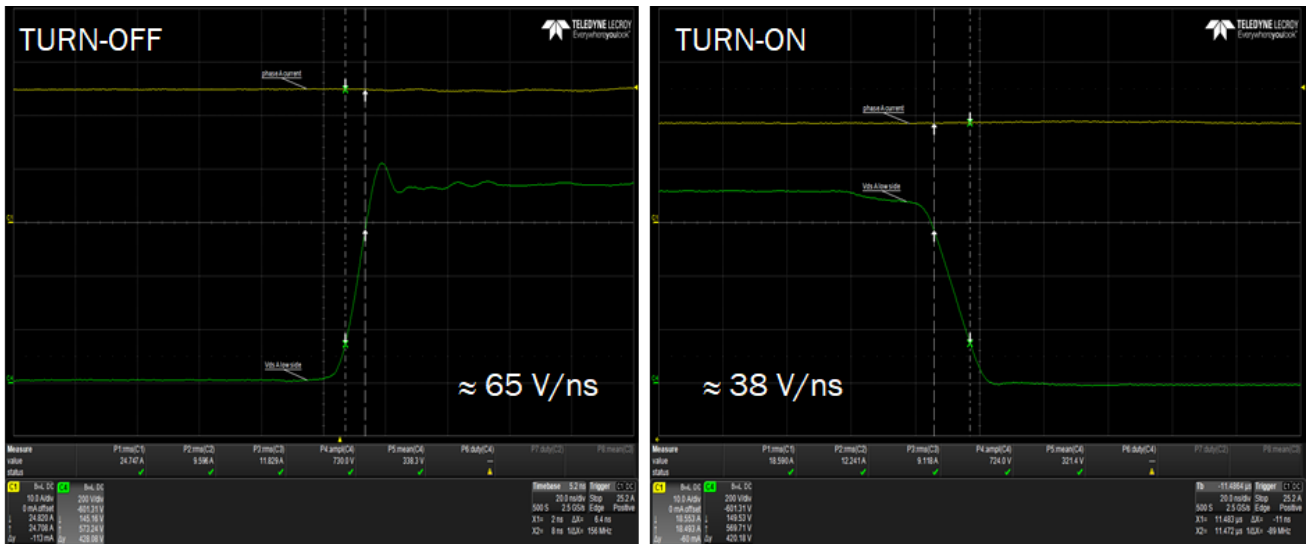
Figure 8. Switching Speed Low Side SiC MOSFET

Different PWM strategies implemented and tested. Each of them affects the inductor high frequency current ripple while the low frequency envelope follows the output target power. Although the current ripple is linked to the PWM frequency and bus voltage, it is also heavily affected by the zero sequence voltage. Zero sequence voltage affects the voltage generation across the inductor in a PWM period.
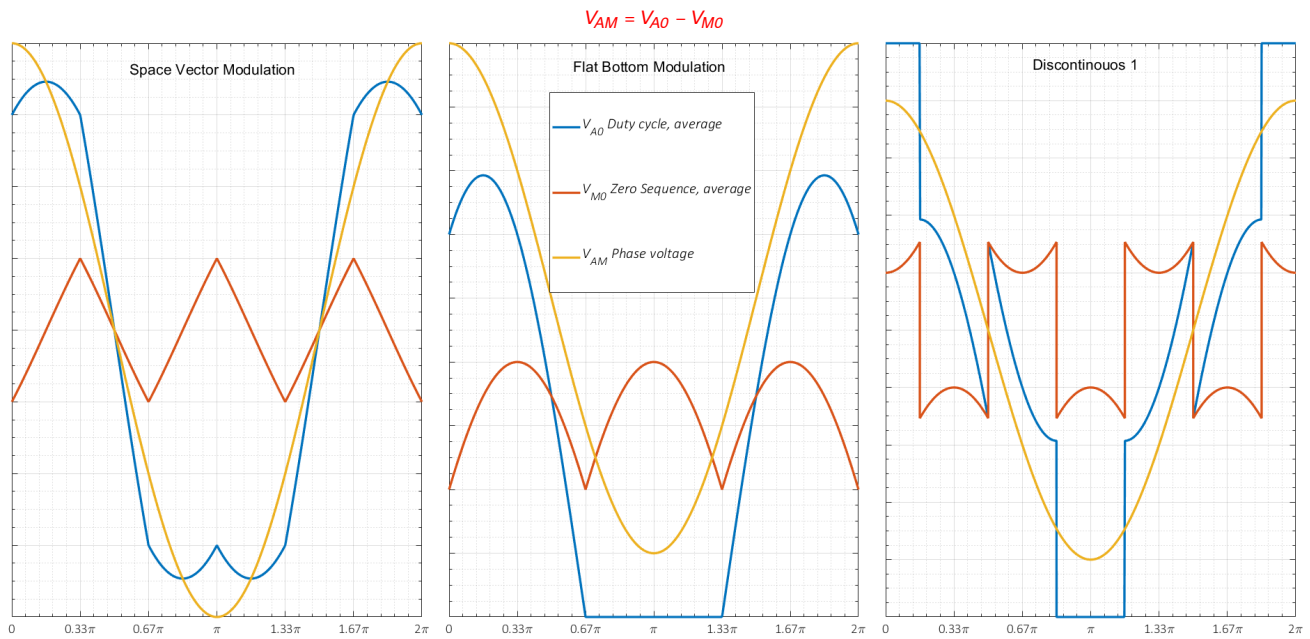

Figure 9. Tested Modulation Strategy

Figure 10. Efficiency Results @ f_{PWM} = 100 kHz

And finally system efficiency results of running the PFC board at 100 kHz selecting the discontinuous type 1 modulation strategy.
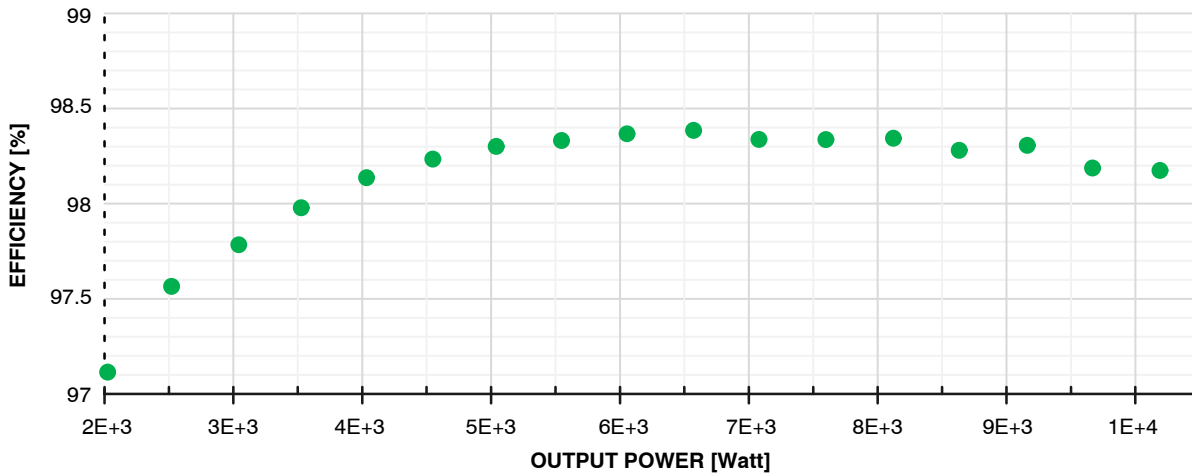
Figure 11. Efficiency Results @ f_{PWM} = 100 kHz

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