

# NCS2564

## Four-Channel Video Driver with Selectable SD / HD Reconstruction Filters

The NCS2564 is a 4-channel high speed video driver with 6th order Butterworth Reconstruction filters on each channel. A first set of 3-channel has selectable Standard Definition (SD) / High Definition (HD) filters, one per channel. A fourth channel offers an extra filter driver for driving CVBS-type video signal. The NCS2564 is in fact a combination of a triple SD/HD video driver plus a single CVBS video driver.

It is designed to be compatible with Digital-to-Analog Converters (DAC) embedded in most video processors.

To further reduce power consumption, 2 enable pins are provided one for the triple driver and another one for the single driver. One pin allows selecting the filter frequency of the triple driver. All channels can accept DC- or AC-coupled signals. In case of AC-coupled inputs, the internal clamps are enabled. The outputs can drive both AC and DC coupled 150  $\Omega$  loads.

### Features

- 3-Channel with per Channel a Selectable Sixth-Order Butterworth 8/34 MHz Filter
- One CVBS Driver Including 6th Order Butterworth 8 MHz Filter
- Transparent Clamp
- Internal Fixed Gain: 6 dB  $\pm$  0.2
- Integrated Level Shifter
- AC- or DC-Coupled Inputs and Outputs
- Low Quiescent Current
- Shutdown Current 42  $\mu$ A Typical (Disabled)
- Each channel Capable to Drive 2 by 150  $\Omega$  Loads
- Wide Operating Supply Voltage Range: +4.7 V to +5.3 V
- 8 kV ESD Protection (IEC61000-4-2 Compatible)
- TSSOP-14 Package
- These are Pb-Free Devices

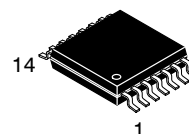
### Typical Application

- Set Top Box Decoder
- DVD Player / Recorder
- HDTV



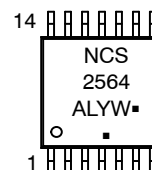
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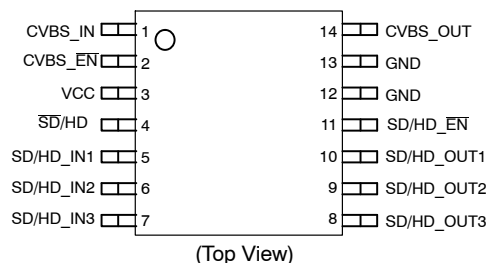
TSSOP-14  
TBD SUFFIX  
CASE 948G

### MARKING DIAGRAM



- NCS2564 = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

### PINOUT



### ORDERING INFORMATION

| Device        | Package               | Shipping†             |
|---------------|-----------------------|-----------------------|
| NCS2564DTBR2G | TSSOP-14<br>(Pb-Free) | 2500 /<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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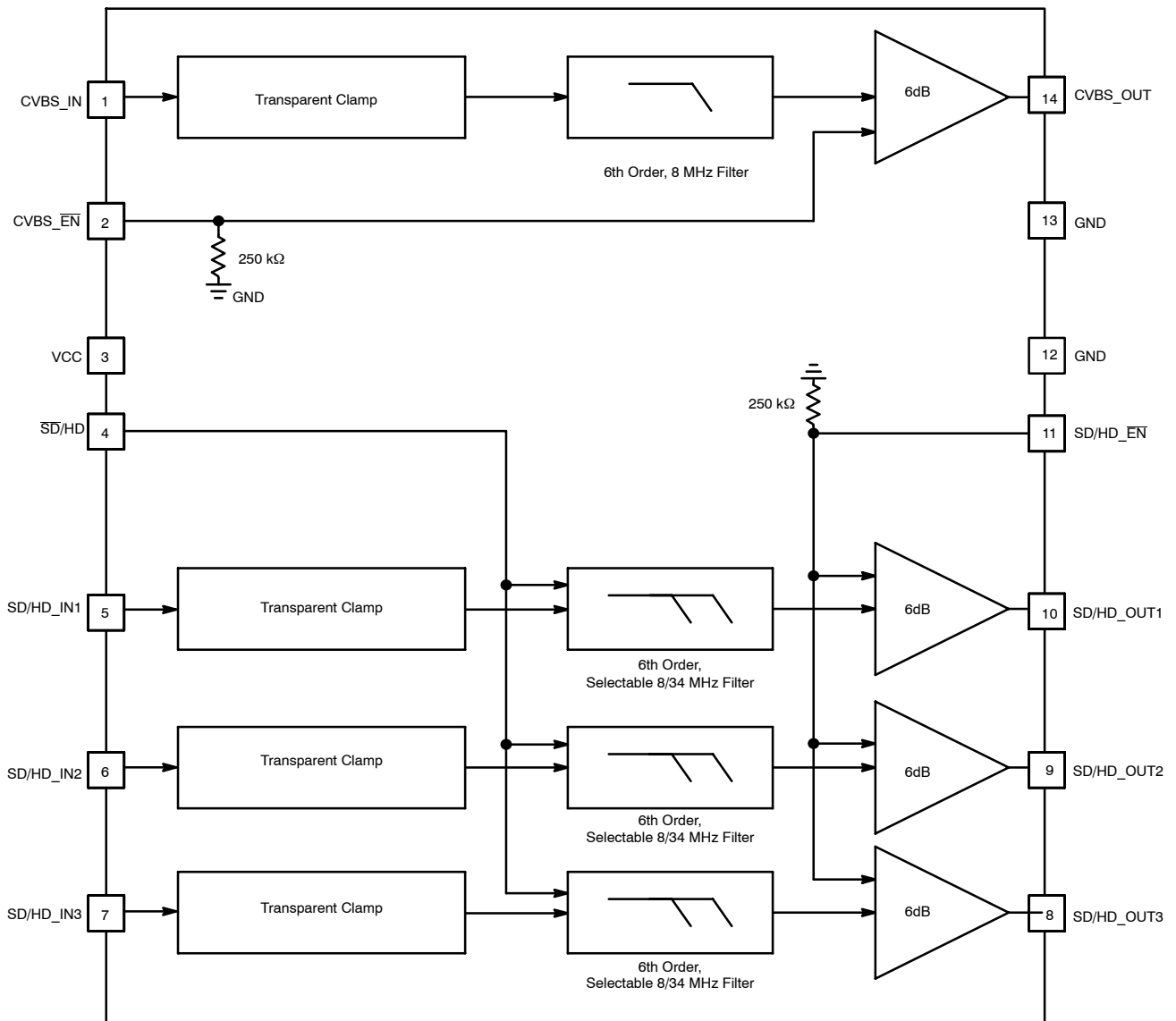


Figure 1. NCS2564 Block Diagram

# NCS2564

## PIN DESCRIPTION

| Pin No. | Name               | Type   | Description   |
|---------|--------------------|--------|---|
| 1       | CVBS_IN            | Input  | Video Input for Video Signal featuring a frequency bandwidth compatible with NTSC / PAL / SECAM Video (8 MHz) – CVBS Channel  |
| 2       | CVBS_EN            | Input  | CVBS Channel Enable /Disable Function: Low = Enable, High = Disable. When left open the default state is Enable.  |
| 3       | VCC                | Power  | Power Supply / 4.7 V to 5.3 V   |
| 4       | $\overline{SD/HD}$ | Input  | Pin of selection enabling the Standard Definition or High Definition Filters (8 MHz / 34 MHz) for channels SD/HD – when Low SD filters are selected, when High HD filters are selected. |
| 5       | SD/HD_IN1          | Input  | Selectable SD or HD Video Input 1 – SD/HD Channel 1   |
| 6       | SD/HD_IN2          | Input  | Selectable SD or HD Video Input 2 – SD/HD Channel 2   |
| 7       | SD/HD_IN3          | Input  | Selectable SD or HD Video Input 3 – SD/HD Channel 3   |
| 8       | SD/HD_OUT3         | Output | SD/HD Video Output 3 – SD/HD Channel 3  |
| 9       | SD/HD_OUT2         | Output | SD/HD Video Output 2 – SD/HD Channel 2  |
| 10      | SD/HD_OUT1         | Output | SD/HD Video Output 1 – SD/HD Channel 1  |
| 11      | SD/HD_EN           | Input  | SD/HD Channel Enable/Disable Function: Low = Enable, High = Disable. When left open the default state is Enable.  |
| 12      | GND                | Ground | Ground  |
| 13      | GND                | Ground | Ground  |
| 14      | CVBS_OUT           | Output | CVBS Video Output – CVBS Channel  |

**MAXIMUM RATINGS**

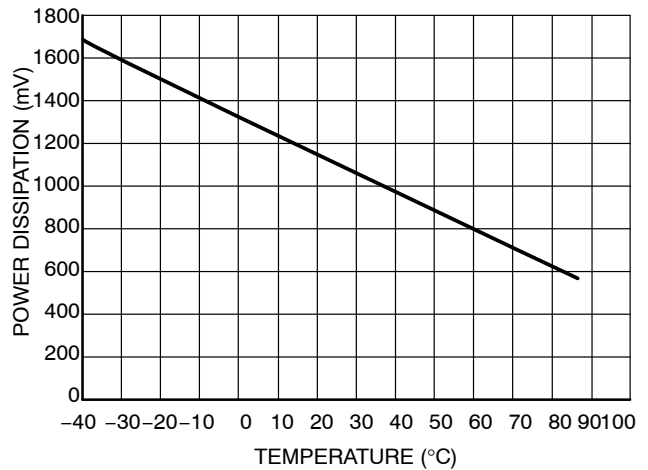
| Rating                                    | Symbol          | Value                       | Unit |
|---|-----------------|-----------------------------|------|
| Power Supply Voltages                     | $V_{CC}$        | $-0.3 \leq V_{CC} \leq 5.5$ | Vdc  |
| I/O Voltage Range                         | $V_{IO}$        | $-0.3 \leq V_I \leq V_{CC}$ | Vdc  |
| Input Differential Voltage Range          | $V_{ID}$        | $-0.3 \leq V_I \leq V_{CC}$ | Vdc  |
| Output Current (Indefinitely) per Channel | $I_O$           | 40                          | mA   |
| Maximum Junction Temperature (Note 1)     | $T_J$           | 150                         | °C   |
| Operating Ambient Temperature             | $T_A$           | -40 to +85                  | °C   |
| Storage Temperature Range                 | $T_{stg}$       | -60 to +150                 | °C   |
| Thermal Resistance, Junction-to-Air       | $R_{\theta JA}$ | 125                         | °C/W |
| ESD Protection Voltage (IEC61000-4-2)     | $V_{esd}$       | >8000                       | V    |
| ESD HBM – Human Body Model                | HBM             | 4000                        | V    |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Power dissipation must be considered to ensure maximum junction temperature ( $T_J$ ) is not exceeded.

**Maximum Power Dissipation**

The maximum power that can be safely dissipated is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 150°C. If the maximum is exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the “overheated” condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves.



**Figure 2. Power Dissipation vs Temperature**

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**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +5.0\text{ V}$ ,  $R_{source} = 37.5\ \Omega$ ,  $T_A = 25^\circ\text{C}$ , inputs AC-coupled with  $0.1\ \mu\text{F}$ , all outputs AC-coupled with  $220\ \mu\text{F}$  into  $150\ \Omega$  referenced to  $400\ \text{kHz}$ ; unless otherwise specified)

| Symbol              | Characteristics                              | Conditions   | Min | Typ      | Max      | Unit          |
|---------------------|--|--|-----|----------|----------|---------------|
| <b>POWER SUPPLY</b> |  |  |     |          |          |               |
| $V_{CC}$            | Supply Voltage Range                         |  | 4.7 | 5.0      | 5.3      | V             |
| $I_{CC}$            | Supply Current                               | SD Channels Selected + $C_{vbs}$<br>HD Channels Selected + $C_{vbs}$ |     | 40<br>50 | 55<br>70 | mA            |
| $I_{SD}$            | Shutdown Current (CVBS_EN and SD/HD_EN High) |  |     | 42       | 60       | $\mu\text{A}$ |

## DC PERFORMANCE

|          |  |  |     |     |          |            |
|----------|--|--|-----|-----|----------|------------|
| $V_i$    | Input Common Mode Voltage Range                  |  | GND |     | 1.4      | $V_{PP}$   |
| $V_{IL}$ | Input Low Level for the Control Pins (2, 4, 11)  |  | 0   |     | 0.8      | V          |
| $V_{IH}$ | Input High Level for the Control Pins (2, 4, 11) |  | 2.4 |     | $V_{CC}$ | V          |
| $R_{pd}$ | Pulldown Resistors on Pins CVBS_EN and SD/HD_EN  |  |     | 250 |          | k $\Omega$ |

## OUTPUT CHARACTERISTICS

|          |                           |  |  |     |  |    |
|----------|---------------------------|--|--|-----|--|----|
| $V_{OH}$ | Output Voltage High Level |  |  | 2.8 |  | V  |
| $V_{OL}$ | Output Voltage Low Level  |  |  | 200 |  | mV |
| $I_O$    | Output Current            |  |  | 40  |  | mA |

**AC ELECTRICAL CHARACTERISTICS FOR STANDARD DEFINITION CHANNELS** (pin numbers (1, 14) (5, 10), (6, 9), (7, 8)) ( $V_{CC} = +5.0\text{ V}$ ,  $V_{in} = 1\text{ V}_{PP}$ ,  $R_{source} = 37.5\ \Omega$ ,  $T_A = 25^\circ\text{C}$ , inputs AC-coupled with  $0.1\ \mu\text{F}$ , all outputs AC-coupled with  $220\ \mu\text{F}$  into  $150\ \Omega$  referenced to  $400\ \text{kHz}$ ; unless otherwise specified,  $\overline{SD/HD} = \text{Low}$ )

| Symbol           | Characteristics                       | Conditions                                     | Min        | Typ        | Max | Unit     |
|------------------|---------------------------------------|--|------------|------------|-----|----------|
| $A_{VSD}$        | Voltage Gain                          | $V_{in} = 1\text{ V}$ – All SD Channels        | 5.8        | 6.0        | 6.2 | dB       |
| $BW_{SD}$        | Low Pass Filter Bandwidth (Note 3)    | -1 dB<br>-3 dB                                 | 5.5<br>6.5 | 7.2<br>8.0 |     | MHz      |
| $A_{RSD}$        | Stop-band Attenuation (Notes 3 and 4) | @ 27 MHz                                       | 43         | 50         |     | dB       |
| $dG_{SD}$        | Differential Gain Error               |  |            | 0.7        |     | %        |
| $d\Phi_{SD}$     | Differential Phase Error              |  |            | 0.7        |     | $^\circ$ |
| THD              | Total Harmonic Distortion             | $V_{out} = 1.4\text{ V}_{PP}$ @ 3.58 MHz       |            | 0.35       |     | %        |
| $X_{SD}$         | Channel-to-Channel Crosstalk          | @ 1 MHz and $V_{in} = 1.4\text{ V}_{PP}$       |            | -57        |     | dB       |
| $SNR_{SD}$       | Signal-to-Noise Ratio                 | NTC-7 Test Signal, 100 kHz to 4.2 MHz (Note 2) |            | 72         |     | dB       |
| $\Delta t_{SD}$  | Propagation Delay                     | @ 4.5 MHz                                      |            | 70         |     | ns       |
| $\Delta GD_{SD}$ | Group Delay Variation                 | 100 kHz to 8 MHz                               |            | 20         |     | ns       |

2.  $SNR = 20 \times \log(714\text{ mV} / \text{RMS noise})$

3. 100% of Tested ICs fit the bandwidth and attenuation tolerance at  $25^\circ\text{C}$ .

4. Guaranteed by characterization.

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### AC ELECTRICAL CHARACTERISTICS FOR HIGH DEFINITION CHANNELS (pin numbers (5, 10) (6, 9), (7, 8))

( $V_{CC} = +5.0\text{ V}$ ,  $V_{in} = 1\text{ V}_{PP}$ ,  $R_{source} = 37.5\ \Omega$ ,  $T_A = 25^\circ\text{C}$ , inputs AC-coupled with  $0.1\ \mu\text{F}$ , all outputs AC-coupled with  $220\ \mu\text{F}$  into  $150\ \Omega$  referenced to 400 kHz; unless otherwise specified,  $\overline{\text{SD}}/\text{HD} = \text{High}$ )

| Symbol           | Characteristics                              | Conditions   | Min      | Typ               | Max | Unit |
|------------------|--|--|----------|-------------------|-----|------|
| $A_{VHD}$        | Voltage Gain                                 | $V_{in} = 1\text{ V}$ – All HD Channels  | 5.8      | 6.0               | 6.2 | dB   |
| $BW_{HD}$        | Low Pass Filter Bandwidth                    | -1 dB (Note 6)<br>-3 dB (Note 7)   | 26<br>30 | 31<br>34          |     | MHz  |
| $A_{RHD}$        | Stop-band Attenuation                        | @ 44.25 MHz (Note 7)<br>@ 74.25 MHz (Note 6)   | 33       | 15<br>42          |     | dB   |
| $THD_{HD}$       | Total Harmonic Distortion                    | $V_{out} = 1.4\text{ V}_{PP}$ @ 10 MHz<br>$V_{out} = 1.4\text{ V}_{PP}$ @ 15 MHz<br>$V_{out} = 1.4\text{ V}_{PP}$ @ 20 MHz |          | 0.4<br>0.6<br>0.8 |     | %    |
| $X_{HD}$         | Channel-to-Channel Crosstalk                 | @ 1 MHz and $V_{in} = 1.4\text{ V}_{PP}$   |          | -60               |     | dB   |
| $SNR_{HD}$       | Signal-to-Noise Ratio                        | White Signal, 100 kHz to 30 MHz,<br>(Note 5)   |          | 72                |     | dB   |
| $\Delta t_{HD}$  | Propagation Delay                            |  |          | 25                |     | ns   |
| $\Delta GD_{HD}$ | Group Delay Variation from 100 kHz to 30 MHz |  |          | 10                |     | ns   |

5.  $SNR = 20 \times \log(714\text{ mV} / \text{RMS noise})$

6. Guaranteed by Characterization.

7. 100% of Tested ICs fit the bandwidth and attenuation tolerance at  $25^\circ\text{C}$ .

TYPICAL CHARACTERISTICS

$V_{CC} = +5.0\text{ V}$ ,  $V_{in} = 1\text{ V}_{PP}$ ,  $R_{source} = 37.5\ \Omega$ ,  $T_A = 25^\circ\text{C}$ , Inputs AC-coupled with  $0.1\ \mu\text{F}$ , All Outputs AC-coupled with  $220\ \mu\text{F}$  into  $150\ \Omega$   
 Referenced to 400 kHz; unless otherwise specified

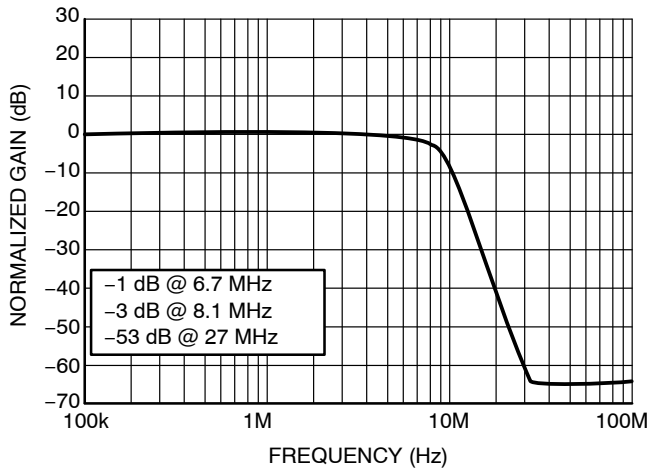


Figure 3. SD Normalized Frequency Response

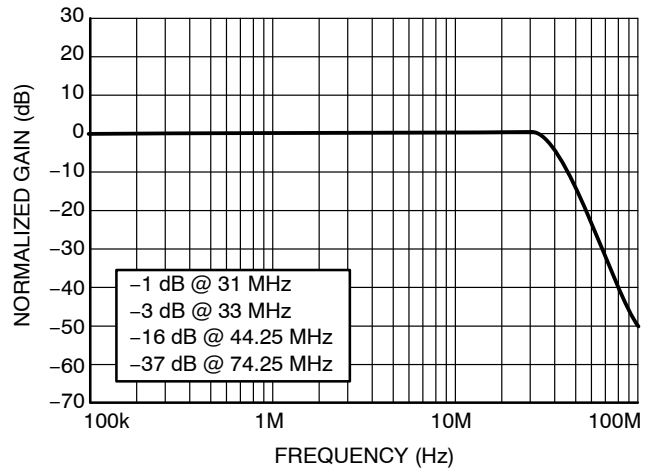


Figure 4. HD Normalized Frequency Response

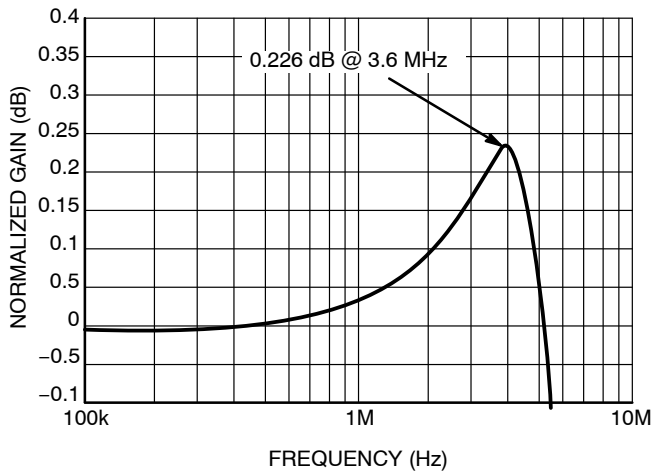


Figure 5. SD Passband Flatness

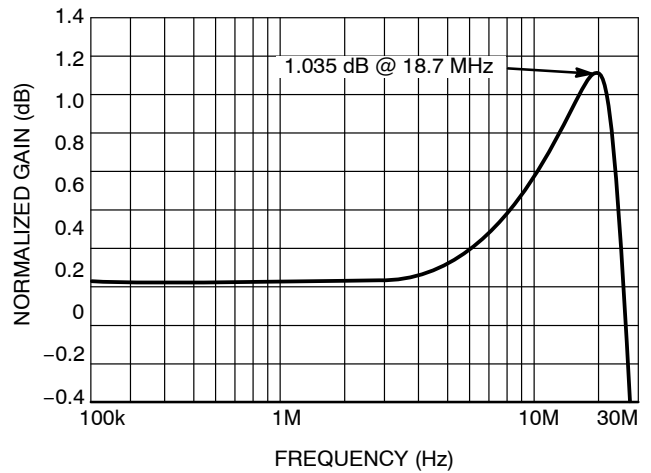


Figure 6. HD Passband Flatness

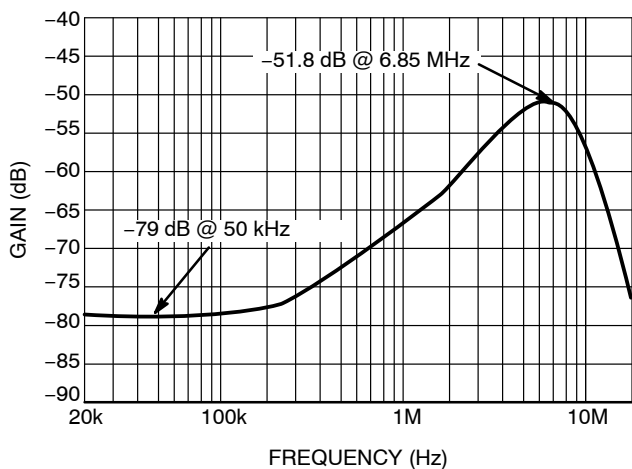


Figure 7. SD Channel-to-Channel Crosstalk

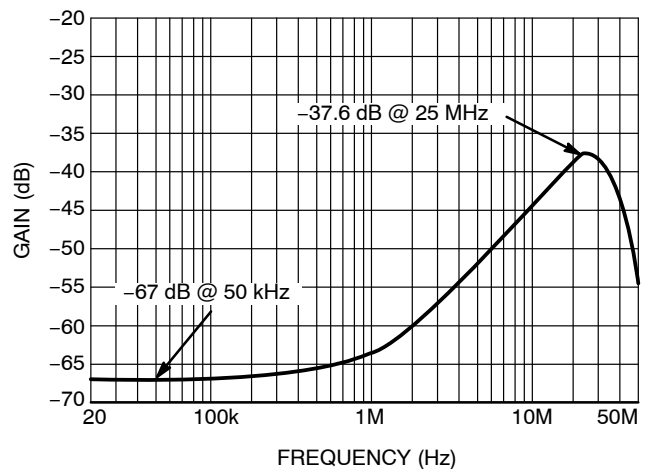


Figure 8. HD Channel-to-Channel Crosstalk

TYPICAL CHARACTERISTICS

$V_{CC} = +5.0\text{ V}$ ,  $V_{in} = 1\text{ V}_{PP}$ ,  $R_{source} = 37.5\ \Omega$ ,  $T_A = 25^\circ\text{C}$ , Inputs AC-coupled with  $0.1\ \mu\text{F}$ , All Outputs AC-coupled with  $220\ \mu\text{F}$  into  $150\ \Omega$   
 Referred to 400 kHz; unless otherwise specified

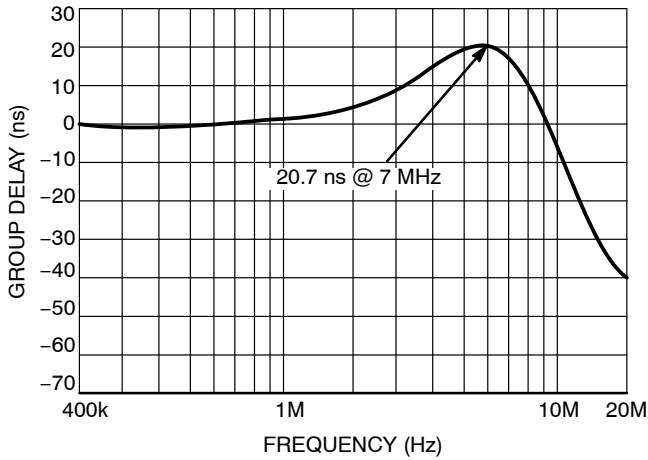


Figure 9. SD Normalized Group Delay

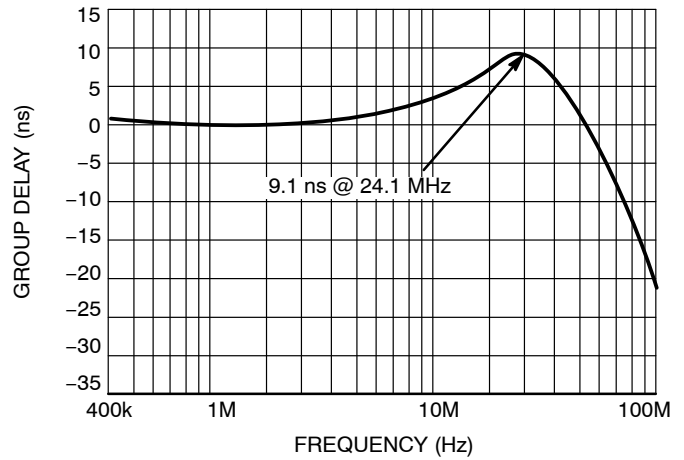


Figure 10. HD Normalized Group Delay

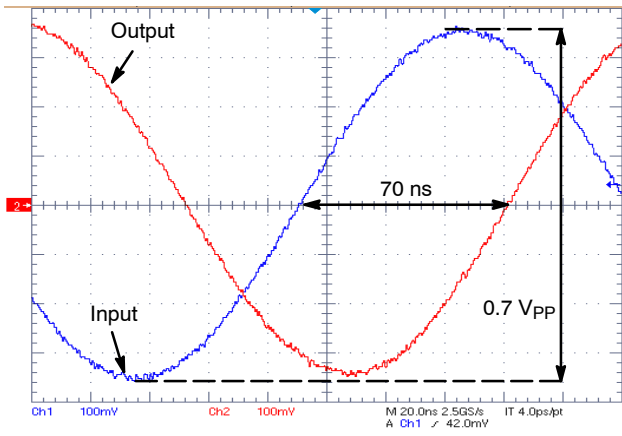


Figure 11. SD Propagation Delay

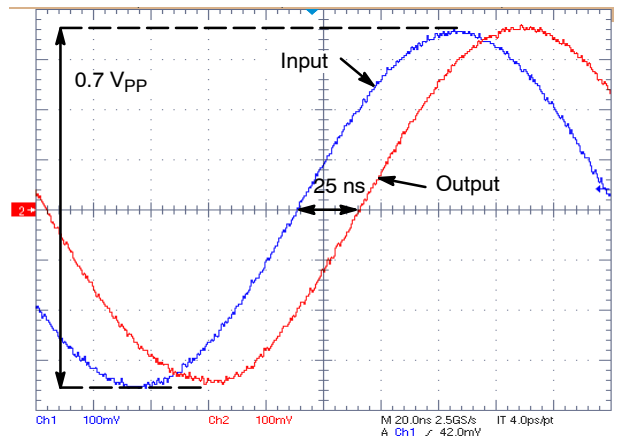


Figure 12. HD Propagation Delay

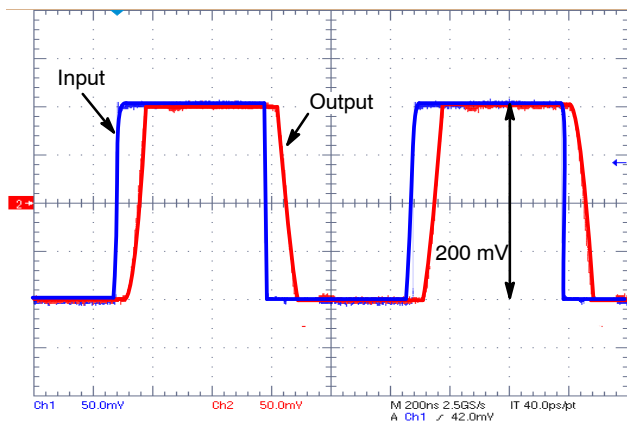


Figure 13. SD Small Signal Response

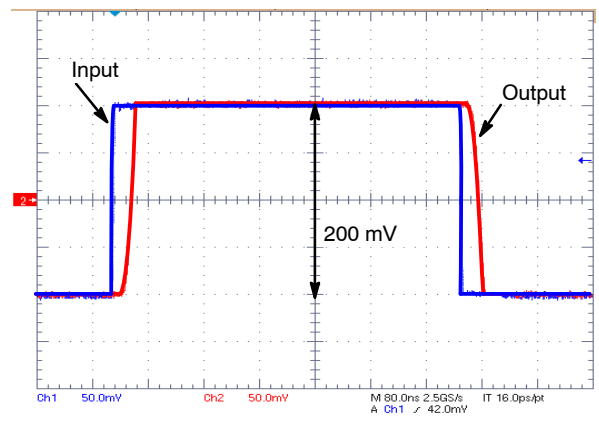


Figure 14. HD Small Signal Response



# NCS2564

## TYPICAL CHARACTERISTICS

$V_{CC} = +5.0\text{ V}$ ,  $V_{in} = 1\text{ V}_{PP}$ ,  $R_{source} = 37.5\ \Omega$ ,  $T_A = 25^\circ\text{C}$ , Inputs AC-coupled with  $0.1\ \mu\text{F}$ , All Outputs AC-coupled with  $220\ \mu\text{F}$  into  $150\ \Omega$   
Referenced to 400 kHz; unless otherwise specified

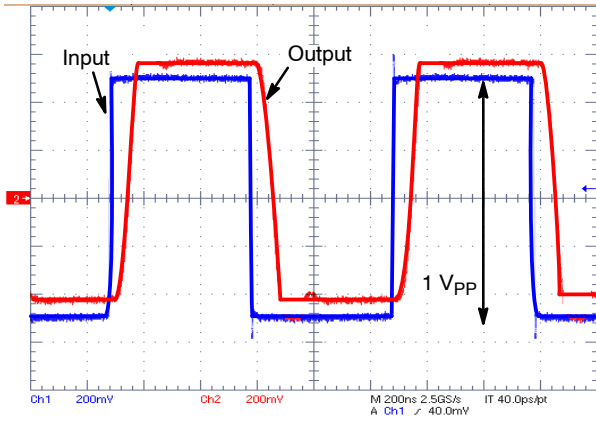


Figure 15. SD Large Signal Response

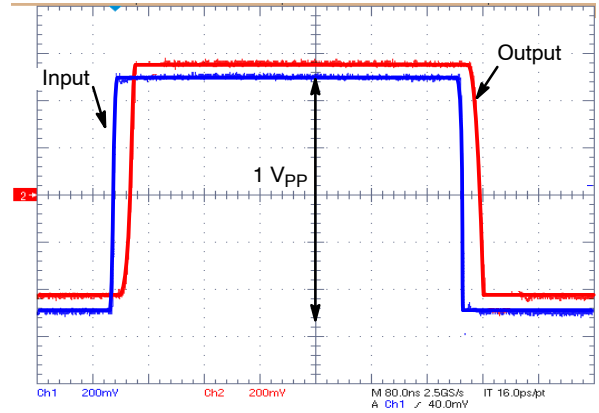


Figure 16. HD Large Signal Response

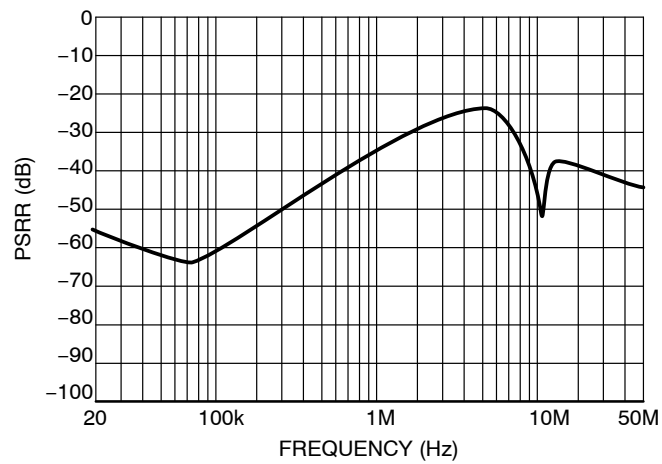


Figure 17. SD and HD  $V_{CC}$  PSRR vs. Frequency

TYPICAL CHARACTERISTICS

$V_{CC} = +5.0\text{ V}$ ,  $V_{in} = 1\text{ V}_{PP}$ ,  $R_{source} = 37.5\ \Omega$ ,  $T_A = 25^\circ\text{C}$ , Inputs AC-coupled with  $0.1\ \mu\text{F}$ , All Outputs AC-coupled with  $220\ \mu\text{F}$  into  $150\ \Omega$   
 Referred to 400 kHz; unless otherwise specified

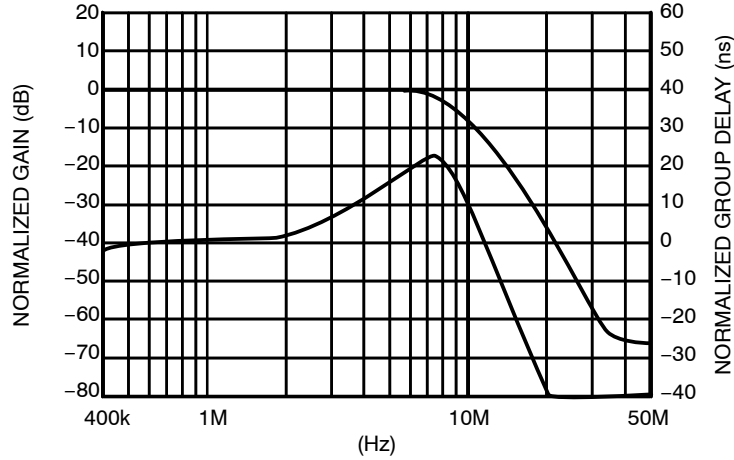


Figure 18. SD Frequency Response and Group Delay

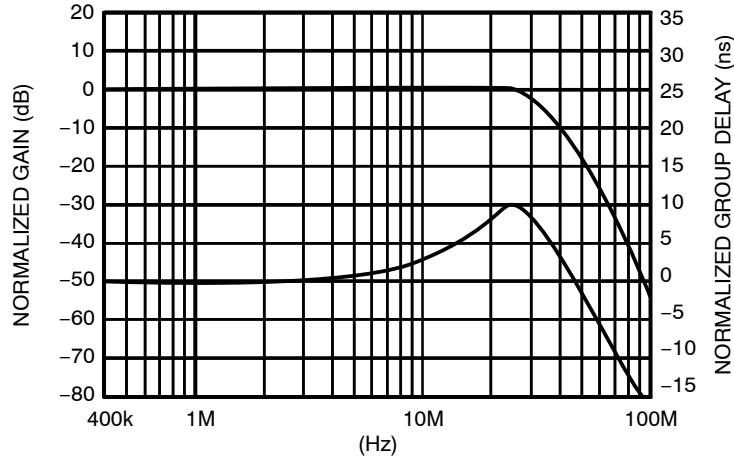


Figure 19. HD Frequency Response and Group Delay

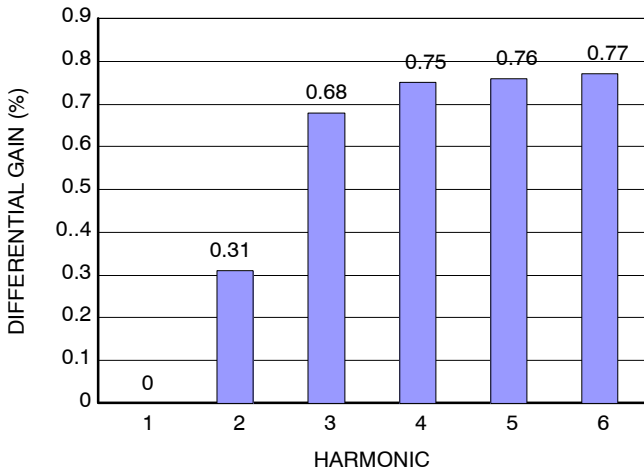


Figure 20. SD Differential Gain

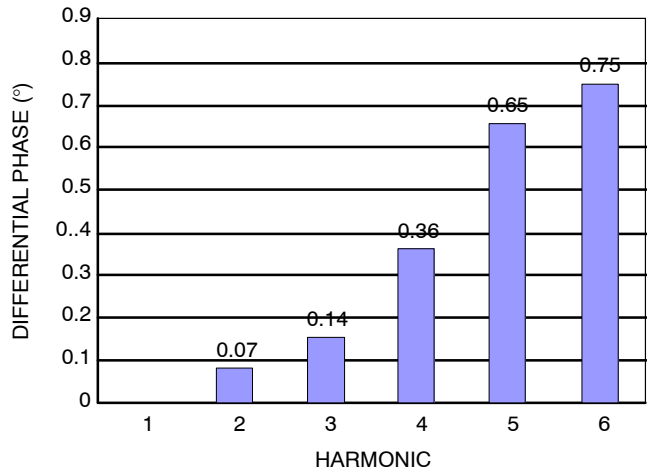


Figure 21. SD Differential Phase

APPLICATIONS INFORMATION

The NCS2564 quad video driver has been optimized for Standard and High Definition video applications covering the requirements of the standards Composite video (CVBS), S-Video, Component Video (480i/525i, 576i/625i, 720p/1080i) and related (RGB). The three SD/HD channels have selectable filters (8 MHz and 34 MHz) for covering either standard definition-like video applications or High Definition video applications. These frequencies are selectable using the pin  $\overline{\text{SD/HD}}$ .

In the regular mode of operation each channel provides an internal voltage-to-voltage gain of 2 from input to output. This effectively reduces the number of external components

required as compared to discrete approached implemented with stand alone op amps. An internal level shifter is employed shifting up the output voltage by adding an offset of 200 mV. This prevents sync pulse clipping and allows DC-coupled output to the 150  $\Omega$  video load. In addition, the NCS2564 integrates a 6<sup>th</sup> order Butterworth filter for each. This allows rejection of the aliases or unwanted over-sampling effects produced by the video DAC. Similarly for the case of DVD recorders which use an ADC, this anti-aliasing filter (reconstruction filter) will avoid picture quality issue and will aid filtration of parasitic signals caused by EMI interference.

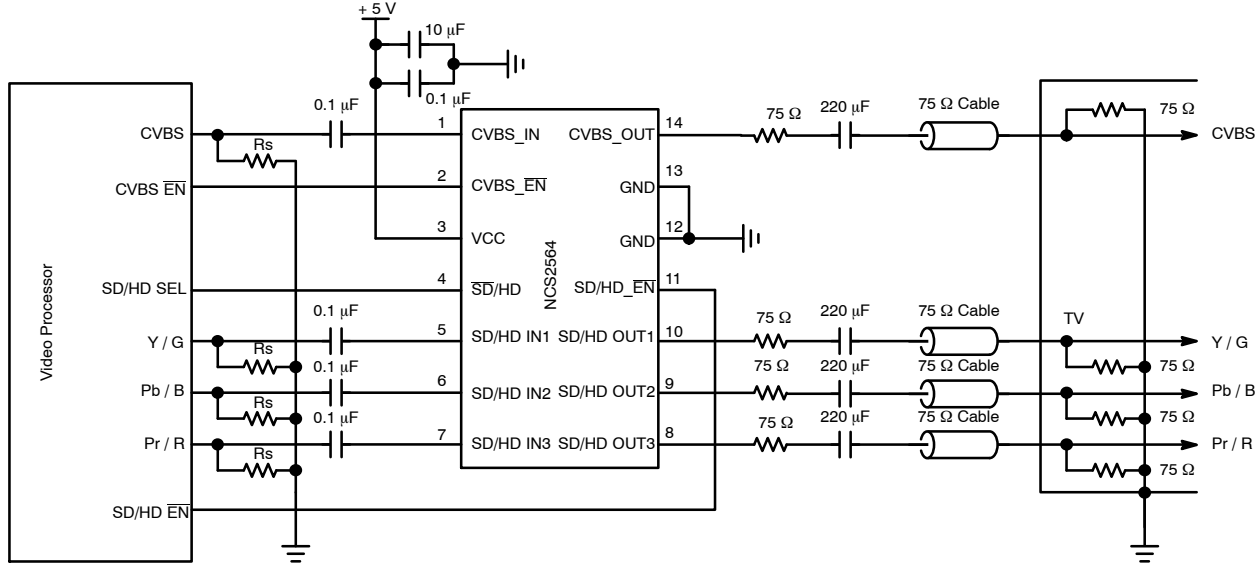


Figure 22. AC-Coupled Configuration at the Input and Output

A built-in diode-like clamp is used into the chip for each channel to support the AC-coupled mode of operation. The clamp is active when the input signal goes below 0 V.

The built-in clamp and level shifter allow the device to operate in different configuration modes depending on the DAC output signal level and the input common mode voltage of the video driver. When the configuration is DC-Coupled at the Inputs and Outputs the 0.1  $\mu\text{F}$  and 220  $\mu\text{F}$  coupling capacitors are no longer used, and the clamps are in that case inactive; this configuration provides a low cost solution which can be implemented with few external components (Figure 23).

The input is AC-coupled when either the input-signal amplitude goes over the range 0 V to 1.4 V or the video source requires such a coupling. In some circumstances it may be necessary to auto-bias signals with the addition of a pullup and pulldown resistors or only pullup resistor (Typical 7.5 M $\Omega$  combined with the internal 800 k $\Omega$  pulldown) making the clamp inactive.

The output AC-coupling configuration is advantageous for eliminating DC ground loop with the drawback of making the device more sensitive to video line or field tilt issues in the case of a too low output coupling capacitor. In

some cases it may be necessary to increase the nominal 220  $\mu\text{F}$  capacitor value.

**Shutdown Mode**

If the enable pins are left open by default the circuit will be enabled. The Enable pin offers a shutdown function, so the NCS2564 can consequently be disabled when not used. The NCS2564's quiescent current reduces to 42  $\mu\text{A}$  typical during shutdown mode.

**DC-Coupled Output**

The outputs of the NCS2564 can be DC-coupled to a 150  $\Omega$  load (Figure 23). This has the advantage of eliminating the AC-coupling capacitors at the output by reducing the number of external components and saving space on the board. This can be a key advantage for some applications with limited space.

The problems of field tilt effects on the video signal are also eliminated providing the best video quality with optimal dynamic or peak-to-peak amplitude of the video signal allowing operating thanks to the built-in level shifter without risk of signal clipping. In this coupling configuration the average output voltage is higher than 0 V and the power consumption can be a little higher than with an AC-coupled configuration.

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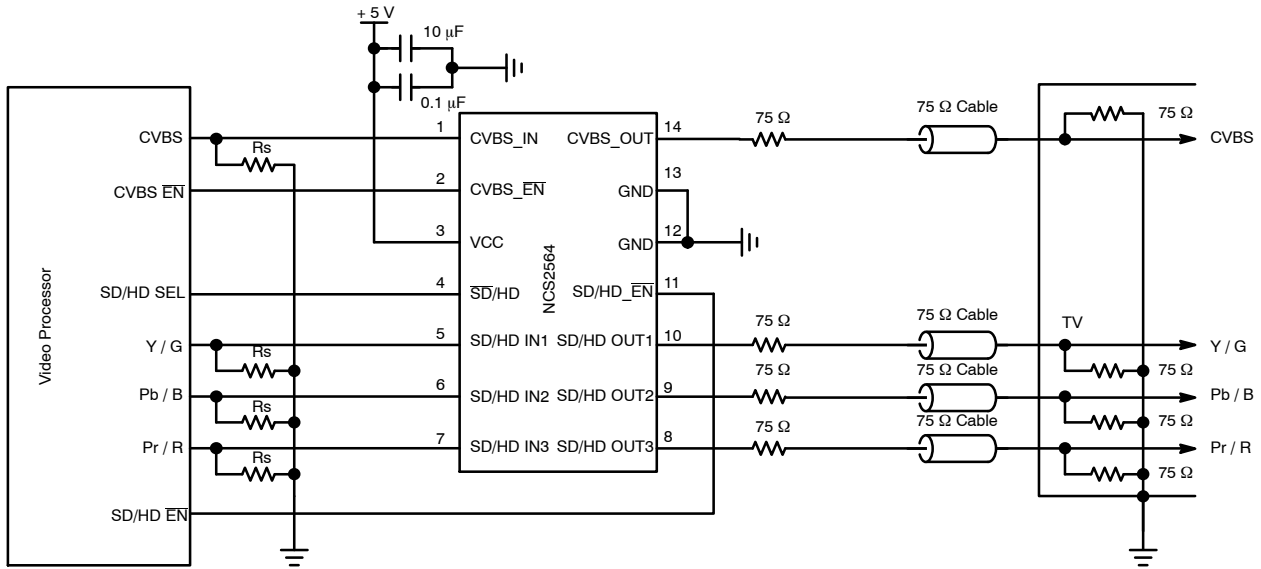


Figure 23. DC-Coupled Input and Output Configuration

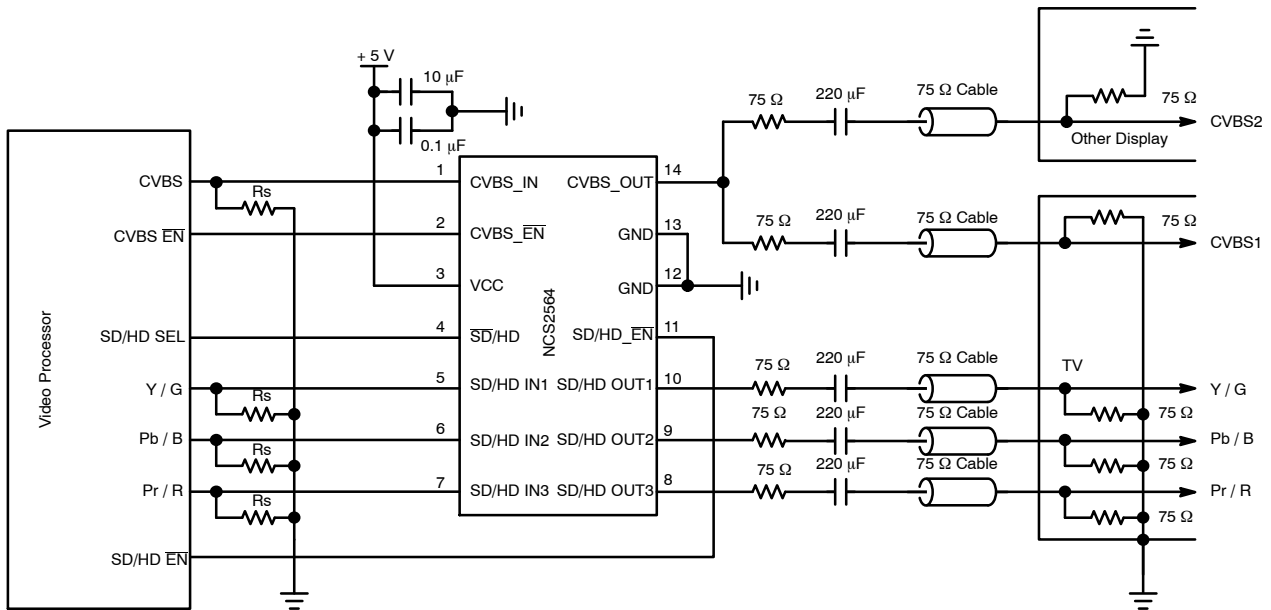


Figure 24. Typical Application

# NCS2564

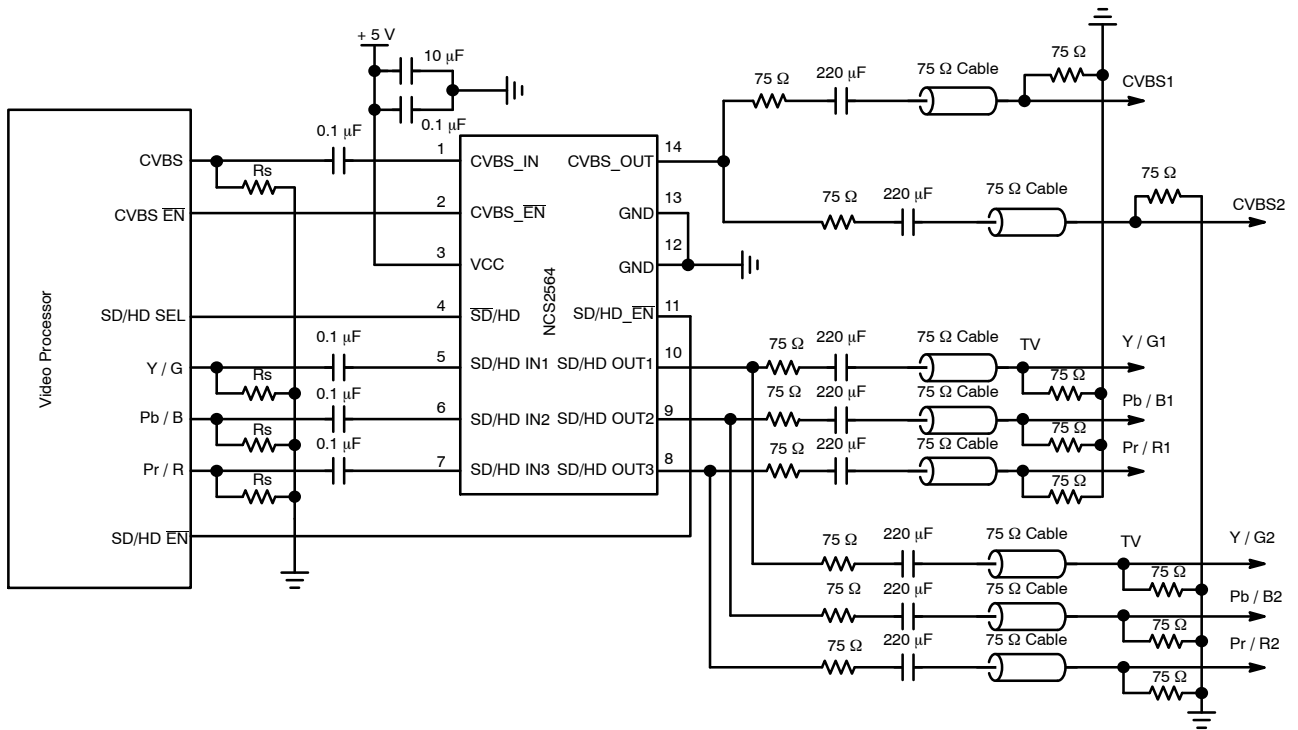


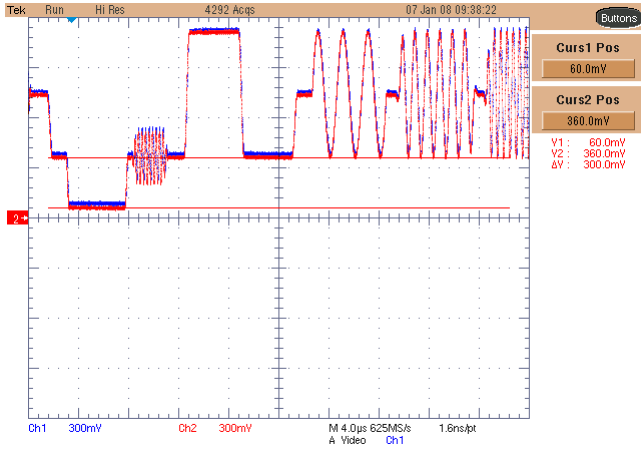
Figure 25. NCS2564 Driving 2 SCARTS Simultaneously

**Video Driving Capability**

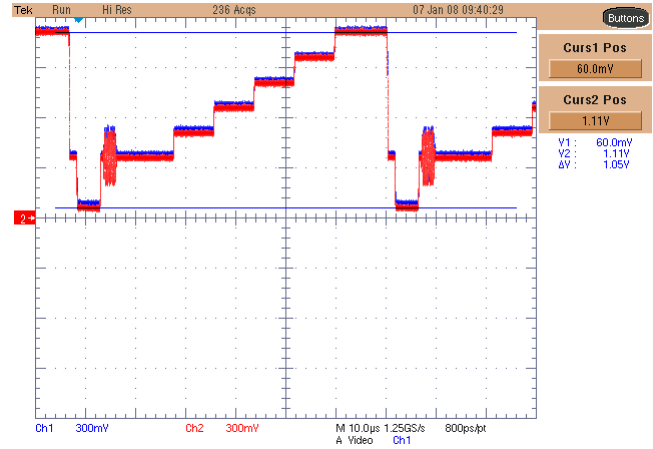
With an output current capability of 40 mA the NCS2564 was designed to be able to drive at least 2 video display loads in parallel. This type of application is illustrated Figure 24. Figure 26 (multiburst) and Figure 27 (linearity) show that the video signal can efficiently drive a 75 Ω equivalent load and not degrade the video performance.

**ESD Protection**

All the device pins are protected against electrostatic discharge at a level of 4 kV HBM and 8 kV according to IEC61000-4-2. This feature has been considered with a particular attention with ESD structure able to sustain the typical values requested by the systems like Set Top Boxes or Blue-Ray players. This parameter is particularly important for video driver which usually constitutes the last stage in the video chain before the video output connector. The IEC61000-4-2 standard has been used to test our devices in the real application environment. Test methodology can be provided on request.



**Figure 26. Multiburst Test with Two 150 Ω Loads**



**Figure 27. Linearity Test with Two 150 Ω Loads**

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