3.3 V OmniClock Generator with Single Ended LVCMOS Output

NB3H60113GH2

WDFN8
CASE 511AT

The NB3H60113GH2, which is a member of the OmniClock family, is a low power PLL−based clock generator. The device accepts a single ended LVCMOS reference clock as input. It generates one single ended LVCMOS modulated output at CLKOUT. Two LVCMOS spread select signals SS1% and SS0% select one of the four spread spectrum options at the output. The device can be powered down using the Power Down pin (PD#).

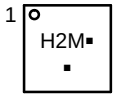
Features

- Member of the OmniClock Family of Programmable Clock Generators
- Operating Power Supply: 3.3 V ±10%
- I/O Standards:
  - Input: 100 MHz CLKIN
  - Output: 100 MHz Modulated CLKOUT (LVCMOS)
- Input Frequency Range:
  - Reference Clock: 100 MHz (LVCMOS)
- Configurable Spread Spectrum Frequency Modulation Parameters (Type, Deviation, Rate)
- Output Drive Current for Single Ended Output: 16 mA
- Power Saving Mode through Power Down Pin
- Temperature Range −40°C to 85°C
- Packaged in 8−Pin WDFN
- These are Pb−Free Devices

Typical Applications

- Display (TV Wall)

MARKING DIAGRAM



H2 = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

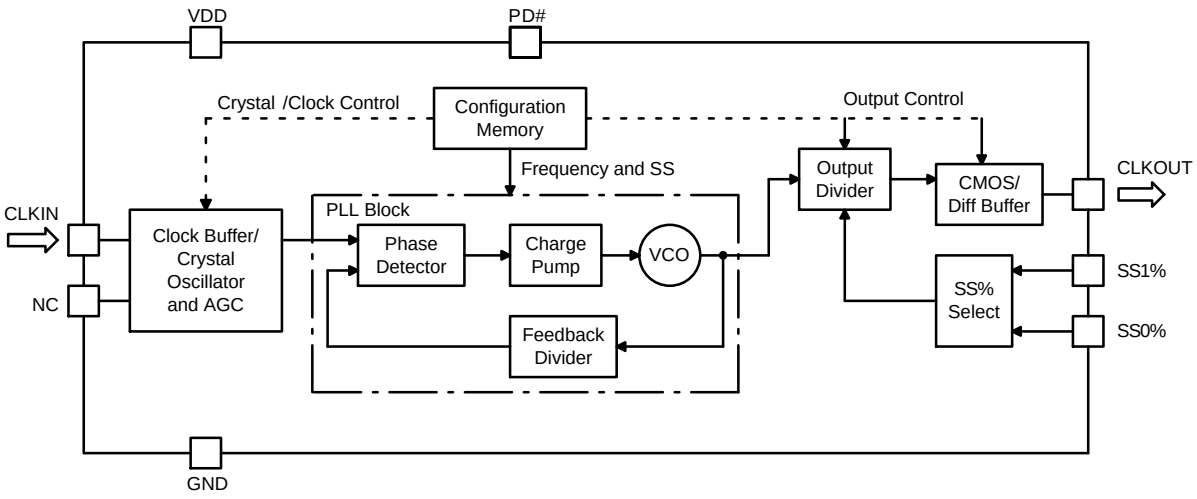


Figure 1. Simplified Block Diagram

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PIN FUNCTION DESCRIPTION

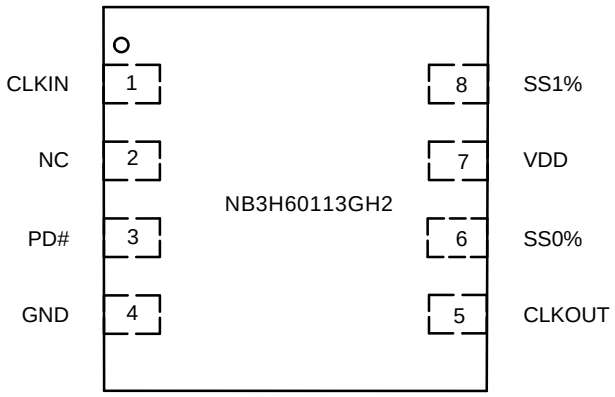


Figure 2. Pin Connections (Top View) – WDFN8

Table 1. PIN DESCRIPTION

Pin No.	Pin Name	Pin Type	Description
1	CLKIN	Input	100 MHz single ended external reference input clock (LVCMOS)
2	NC	Output	No connect. Not to be connected to any circuit
3	PD#	Input	Asynchronous LVCMOS input. Active Low Master Reset to disable the device and set output Low. Internal pull−down resistor. This pin needs to be pulled High for normal operation of the chip.
4	GND	Ground	Power supply ground
5	CLKOUT	Output	100 MHz Modulated Clock Output Single ended (LVCMOS)
6	SS0%	Input	SS% Selection Input (LVCMOS). Default Pin High
7	V_{DD}	Power	3.3 V Power supply
8	SS1%	Input	SS% Selection Input (LVCMOS). Default Pin High

Table 2. POWER DOWN FUNCTION TABLE

PD#	Function
0	Device Powered Down
1	Device Powered Up

Table 3. SPREAD SELECTION

SS1%	SS0%	SS% (±)
0	0	0.125
0	1	1.0
1	0	0.5
1	**1**	**0.375***

*SS1% = 1, SS0% = 1 is the default condition.

FUNCTIONAL DESCRIPTION

The NB3H60113GH2 is a 3.3 V programmable, single ended clock generator, designed to meet the clock requirements for consumer and portable markets. It has a small package size and it requires low power during operation and while in standby. The One−Time Programmable memory allows programming and storing of one configuration in the memory space.

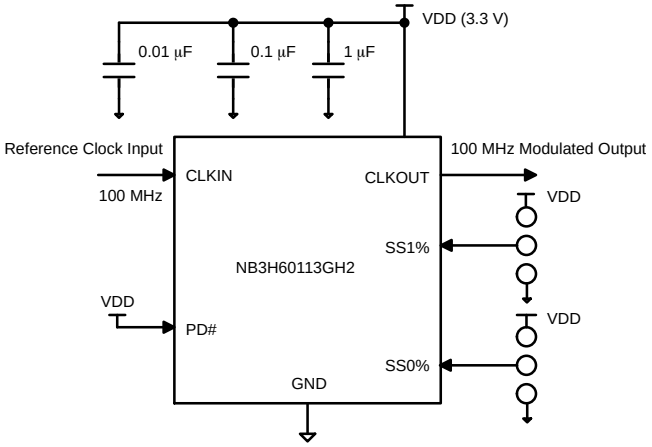


Figure 3. Power Supply Noise Suppression and Typical Application Setup

Device Power Supply

The NB3H60113GH2 is designed to work with a 3.3 V V_{DD} power supply. In order to suppress power supply noise it is recommended to connect decoupling capacitors of 0.1 μF and 0.01 μF close to the V_{DD} pin as shown in Figure 3.

Clock Input: Input Frequency

The NB3H60113GH2 clock input block is programmed for a single ended reference clock source of 100 MHz.

Automatic Gain Control (AGC)

The Automatic Gain Control (AGC) feature adjusts the gain to the input clock based on its signal strength to maintain a good quality input clock signal level. This feature takes care of low clock swings fed from external reference clocks and ensures proper device operation.

Programmable Clock Output: Output Type and Frequency

The NB3H60113GH2 provides one single−ended LVCMOS output of 100 MHz with frequency modulation.

Spread Spectrum Frequency Modulation

Spread spectrum is a technique using frequency modulation to achieve lower peak electromagnetic interference (EMI). It is an elegant solution compared to techniques of filtering and shielding. Refer Figure 4. The NB3H60113GH2 modulates the output of its PLL in order to “spread” the bandwidth of the synthesized clock, decreasing the peak amplitude at the center frequency and at the frequency’s harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum modulation’. The outputs of the NB3H60113GH2 has been programmed to have center spread from ±0.125% to ±1% The programmable step size for spread spectrum deviation is 0.125% for center spread. Additionally, the frequency modulation rate is also programmable. Frequency modulation of 100 kHz has been selected. Spread spectrum, when on, applies to all the outputs of the device. There exists a tradeoff between the input clock frequency and the desired spread spectrum profile.

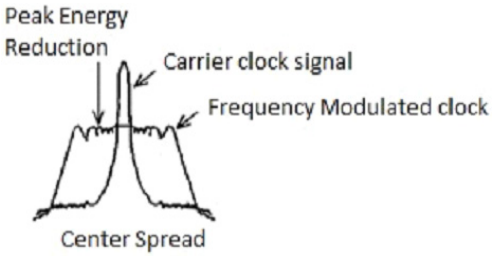


Figure 4.

Control Inputs

Power Down

Power saving mode can be activated through the power down PD# input pin. This input is an LVCMOS/LVTTL active Low Master Reset that disables the device and sets outputs Low. By default it has an internal pull−down resistor. The chip functions are disabled by default and when PD# pin is pulled high the chip functions are activated. Refer Figure 8.

Configuration Space

NB3H60113GH2 has one Configuration. Table 4 shows the device configuration.

Table 4. DEVICE CONFIGURATION

Input Frequency	Output Frequency	V_{DD}	SS%	SS Mod Rate	Output Drive	Output Inversion	Output Enable
100MHz	CLK0 = 100 MHz	3.3 V	±0.375	100 kHz	CLK0 = 16 mA	CLK0 = N	CLK0 = Y

Table 5. ATTRIBUTES

Characteristics	Value
ESD Protection Human Body Model	2 kV
Internal Input Default State Pull Up/Down Resistor	50 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)	MSL1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	130 k
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 6. ABSOLUTE MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Rating	Unit
V_{DD}	Positive Power Supply with Respect to Ground	−0.5 to +4.6	V
V_I	Input Voltage with Respect to Chip Ground	−0.5 to V_{DD} + 0.5	V
V_{OUT}	Output Voltage with Respect to Chip Ground	−0.5 to V_{DD} + 0.5	V
T_A	Operating Ambient Temperature Range (Industrial Grade)	−40 to +85	°C
T_{STG}	Storage Temperature	−65 to +150	°C
T_{SOL}	Max. Soldering Temperature (10 s)	265	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3) 0 lfpm 500 lfpm	 129 84	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	35 to 40	°C/W
T_J	Junction Temperature	125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power). ESD51.7 type board. Back side Copper heat spreader area 100 mm^2, 2 oz (0.070 mm) copper thickness.

Table 7. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Core Power Supply Voltage	3.3 V operation	2.97	3.3	3.63	V
C_L	Clock Output Load Capacitance for LVCMOS Clock	f_{out} < 100 MHz f_{out} ≥ 100 MHz	− −	− −	15 5	pF
fclkin	Reference Clock Frequency	Single ended clock Input	−	100	−	MHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 8. DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V ±10%, GND = 0 V, T_A = −40°C to 85°C, Notes 4, 5)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{DD\_3.3V}$	Power Supply Current for Core	Configuration Dependent. V_{DD} = 3 V, T_A = 25°C, CLKIN = 100 MHz, CLKOUT = 100 MHz, 16 mA output drive	−	25	−	mA
I_{PD}	Power Down Supply Current	PD# is Low to make all outputs OFF, SS default	−	−	20	μA
V_{IH}	Input HIGH Voltage	Pin XIN	0.65 V_{DD}	−	V_{DD}	V
		Pin PD#	0.85 V_{DD}	−	V_{DD}	
V_{IL}	Input LOW Voltage	Pin XIN	0	−	0.35 V_{DD}	V
		Pin PD#	0	−	0.15 V_{DD}	
Zo	Nominal Output Impedance	Configuration Dependent. 16 mA drive	−	22	−	Ω
$R_{PUP/PD}$	Internal Pull Up/ Pull Down Resistor	V_{DD} = 3.3 V	−	50	−	kΩ
Cin	Input Capacitance	Pin PD#	−	4	6	pF
LVCMOS OUTPUT						
V_{OH}	Output HIGH Voltage	V_{DD} = 3.3 V, I_{OH} = 16 mA	0.75 V_{DD}	−	−	V
V_{OL}	Output LOW Voltage	V_{DD} = 3.3 V, I_{OL} = 16 mA	−	−	0.25 V_{DD}	V
I_{DD_LVCMOS}	LVCMOS Output Supply Current	Configuration Dependent. T_A = 25°C, CLKOUT = fout in PLL bypass mode, measured on V_{DD} = 3.3 V, f_{out} = 100 MHz, C_L = 5 pF	−	6.5	−	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Measurement taken with single ended clock outputs terminated with test load capacitance of 5 pF and 15 pF. See Figure 5. Specification for LVTTL are valid for the V_{DD} 3.3 V only.
5. Parameter guaranteed by design verification not tested in production.

Table 9. AC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3 V ±10%, GND = 0 V, T_A = −40°C to 85°C, Notes 6, 8 and 9)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
fout	Single Ended Output Frequency		−	100	−	MHz
f_{MOD}	Spread Spectrum Modulation Rate	fclkin ≥ 6.75 MHz	−	100	−	kHz
SS	Percent Spread Spectrum (deviation from nominal frequency)	Center Spread	−	±0.375	−	%
SSstep	Percent Spread Spectrum Change Step Size	Center Spread step size	−	0.125	−	%
t_{PU}	Stabilization Time from Power−up	V_{DD} = 3.3 V with Frequency Modulation	−	3.0	−	ms
t_{PD}	Stabilization Time from Power Down	Time from falling edge on PD# pin to tri−stated outputs (Asynchronous)	−	3.0	−	ms
Eppm	Synthesis Error	Configuration Dependent	−	0	−	ppm

Table 9. AC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3 V ±10%, GND = 0 V, T_A = −40°C to 85°C, Notes 6, 8 and 9)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SINGLE ENDED OUTPUTS						
$t_{JITTER-3.3V}$	Period Jitter Peak−to−Peak	Configuration Dependent. 100 MHz CLKIN input, f_{out} = 100 MHz, SS min (±0.125) (Notes 7, 9 and 10, see Figure 7)	−	90	−	ps
	Cycle−Cycle Peak Jitter	Configuration Dependent. 100 MHz CLKIN input, f_{out} = 100 MHz, SS default (Notes 7, 9 and 10, see Figure 7)	−	60	−	
tr/tf	Rise/Fall Time	Measured between 20% to 80% with 15 pF load, f_{out} = 100 MHz, V_{DD} = 3.3V, Max Drive	−	1	−	ns
t_{DC}	Output Clock Duty Cycle	V_{DD} = 3.3V Duty Cycle of Ref clock is 50% Reference Clock	40	50	60	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Measurement taken with single ended clock outputs terminated with test load capacitance of 5 pF and 15 pF. See Figure 5. Specification for LVTTL are valid for the V_{DD} 3.3 V only.
7. Measurement taken from single−ended waveform.
8. Parameter guaranteed by design verification not tested in production.
9. AC performance parameters like jitter change based on the output frequency, spread selection, power supply and loading conditions of the output. For application specific AC performance parameters, please contact **onsemi**.
10. Period jitter Sampled with 10,000 cycles, Cycle−cycle jitter sampled with 1,000 cycles. Jitter measurement may vary. Actual jitter is dependent on Input jitter and edge rate, number of active outputs, inputs and output frequencies, supply voltage, temperature, and output load.

PARAMETER MEASUREMENT TEST CIRCUITS

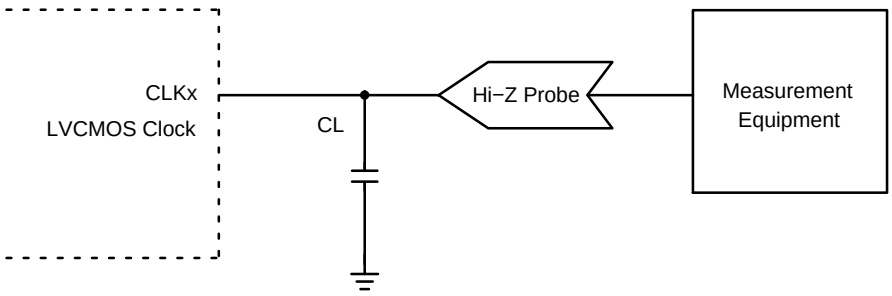


Figure 5. LVCMOS Parameter Measurement

TIMING MEASUREMENT DEFINITIONS

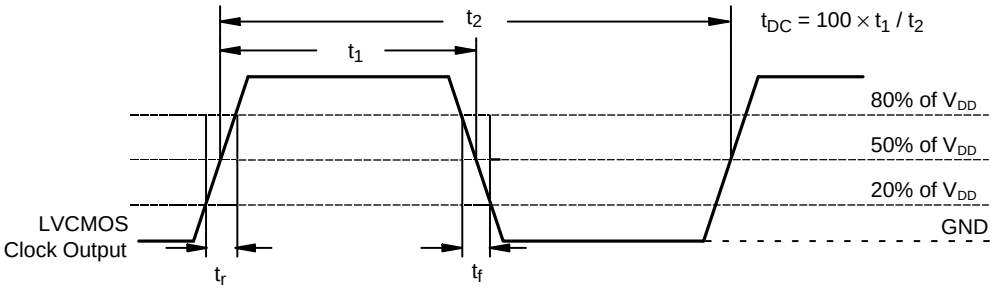


Figure 6. LVCMOS Measurement for AC Parameters

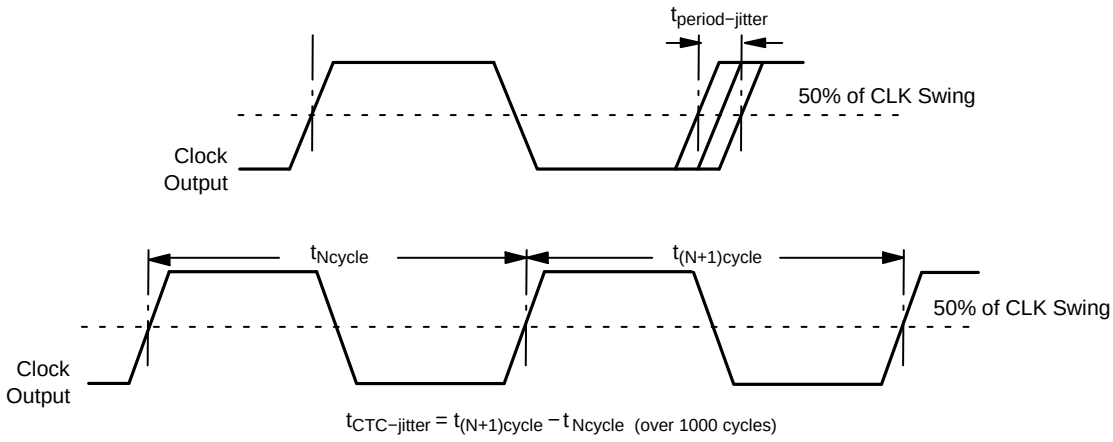


Figure 7. Period and Cycle−Cycle Jitter Measurement

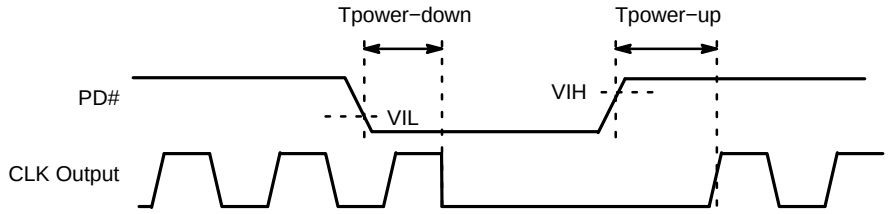


Figure 8. Output Enable/Disable and Power Down Functions

APPLICATION GUIDELINES

LVCMOS Interface

LVCMOS output swings rail−to−rail up to V_{DD} supply and can drive up to 15 pF load at max 16 mA. The NB3H60113GH2 is programmed for max drive of 16 mA. The load current consists of the static current component (varies with drive) and dynamic current component. For any supply voltage, the dynamic load current range per LVCMOS output can be approximated by formula:

$$I_{DD} = f_{out} \cdot C_{load} \cdot V_{DD} \qquad \text{(eq. 1)}$$

C_{load} includes the load capacitor connected to the output, the pin capacitor posed by the output pin (typically 5 pF) and the cap load posed by the receiver input pin.

$$C_{load} = (C_L + C_{pin} + C_{in}) \qquad \text{(eq. 2)}$$

Output Interface and Terminations

The NB3H60113GH2 consists of a unique Single ended Output Driver to support LVCMOS standard. Termination as required must be considered and taken care of by the system designer. An optional series resistor Rs can be connected at the output for impedance matching, to limit the overshoots and ringing.

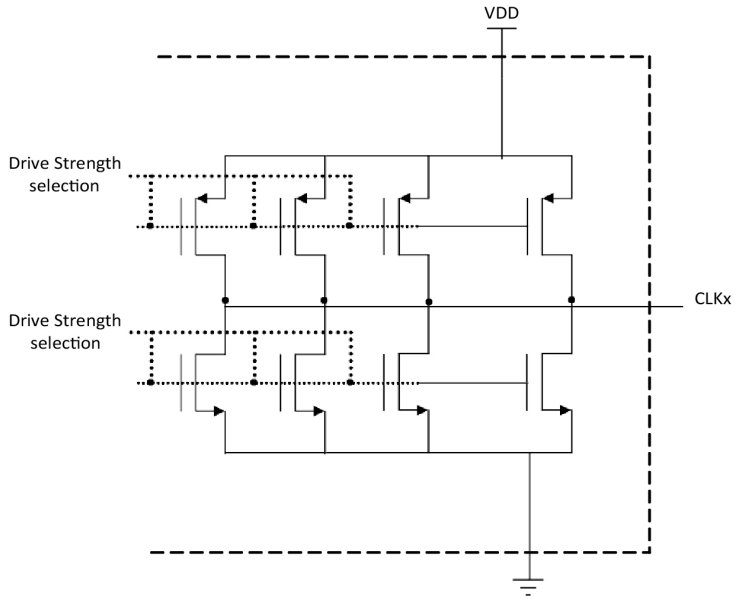


Figure 9. Simplified LVCMOS Output Structure

Field Programming Kit and Software

The NB3H60113GH2 is programmed using the ‘Clock Cruiser Programmable Clock Kit’. This device uses the 8L daughter card on the hardware kit. To design a new clock, ‘Clock Cruiser Software’ is required to be installed from the **onsemi** website. The user manuals for the hardware kit Clock Cruiser Programmable Clock Kit and Clock Cruiser Software can be found following the link www.onsemi.com.

Recommendation for Clock Performance

Clock performance is specified in terms of Jitter in time domain and Phase noise in frequency domain.

Details and measurement techniques of Cycle−cycle jitter, period jitter, TIE jitter and Phase Noise are explained in application note AND8459/D. In order to have a good clock signal integrity for minimum data errors, it is necessary to reduce the signal reflections. Reflection coefficient can be zero only when the source impedance equals the load impedance. Reflections are based on signal transition time (slew rate) and due to impedance mismatch. Impedance matching with proper termination is required to reduce the signal reflections. The amplitude of overshoots is due to the difference in impedance and can be minimized by adding a series resistor (Rs) near the output pin. Greater the difference in impedance, greater is the amplitude of the overshoots and subsequent ripples. The ripple frequency is dependent on the signal travel time from the receiver to the source. Shorter traces results in higher ripple frequency, as the trace gets longer the travel time increases, reducing the ripple frequency. The ripple frequency is independent of signal frequency, and only depends on the trace length and the propagation delay.

For eg. on an FR4 PCB with approximately 150 ps/inch of propagation rate, on a 2 inch trace, the ripple frequency = 1/(150 ps × 2 inch × 5) = 666.6 MHz; [5 = number of times the signal travels, 1 trip to receiver plus 2 additional round trips] PCB traces should be terminated when trace length tr/f / (2 × tprate); tr/f = rise/fall time of signal, tprate = propagation rate of trace.

PCB Design Recommendation

For a clean clock signal waveform it is necessary to have a clean power supply for the device. The device must be isolated from system power supply noise. A 0.1 μF and a 2.2 μF decoupling capacitor should be mounted on the component side of the board as close to the V_{DD} pin as possible. No vias should be used between the decoupling capacitor and V_{DD} pin. The PCB trace to V_{DD} pin and the ground via should be kept thicker and as short as possible. All the V_{DD} pins should have decoupling capacitors. Stacked power and ground planes on the PCB should be large. Signal traces should be on the top layer with minimum vias and discontinuities and should not cross the reference planes. The termination components must be placed near the source or the receiver. In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

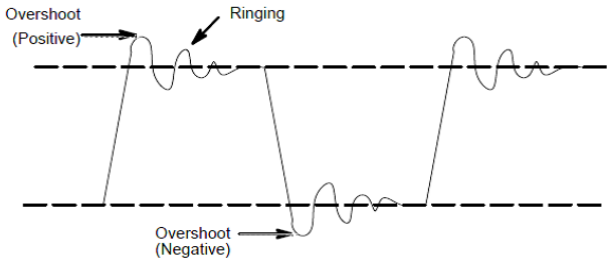


Figure 10. Signal Reflection Components

ORDERING INFORMATION

Part Number	Case	Package	Shipping†
NB3H60113GH2MTR2G	511AT	WDFN8 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

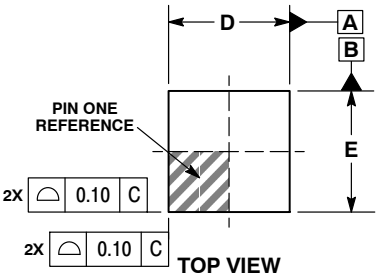
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

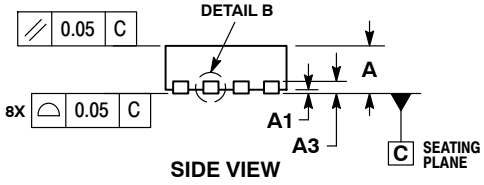
SCALE 4:1

WDFN8 2x2, 0.5P
CASE 511AT−01
ISSUE O

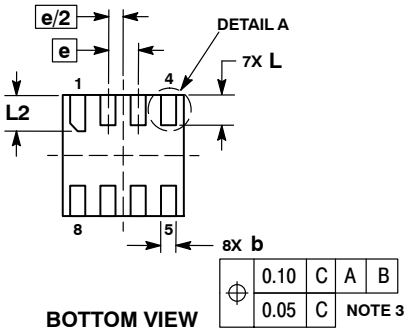
DATE 26 FEB 2010



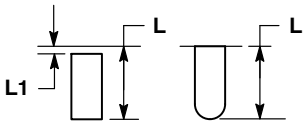
TOP VIEW



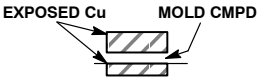
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

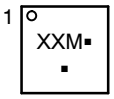


DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

GENERIC MARKING DIAGRAM*

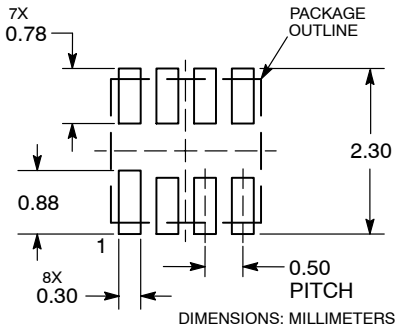


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WDFN8, 2X2, 0.5 P**	**PAGE 1 OF 1**

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