# MC34067, MC33067, NCV33067

# High Performance Resonant Mode Controllers

The MC34067/MC33067 are high performance zero voltage switch resonant mode controllers designed for off−line and dc−to−dc converter applications that utilize frequency modulated constant off−time or constant deadtime control. These integrated circuits feature a variable frequency oscillator, a precise retriggerable one−shot timer, temperature compensated reference, high gain wide bandwidth error amplifier, steering flip−flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of a high speed fault comparator and latch, programmable soft−start circuitry, input undervoltage lockout with selectable thresholds, and reference undervoltage lockout. These devices are available in dual−in−line and surface mount packages.

**Features**

- Zero Voltage Switch Resonant Mode Operation
- Variable Frequency Oscillator with a Control Range Exceeding 1000:1
- Precision One−Shot Timer for Controlled Off−Time
- Internally Trimmed Bandgap Reference
- 4.0 MHz Error Amplifier
- Dual High Current Totem Pole Outputs
- Selectable Undervoltage Lockout Thresholds with Hysteresis
- Enable Input
- Programmable Soft−Start Circuitry
- Low Startup Current for Off−Line Operation
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

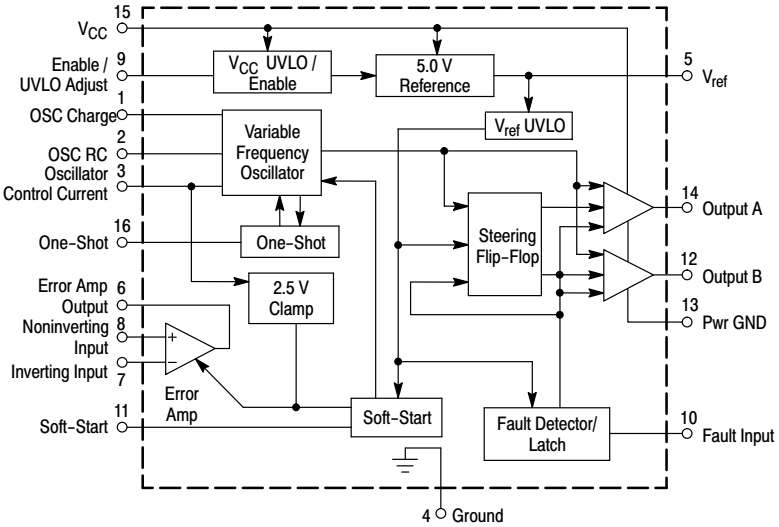


**Figure 1. Simplified Block Diagram**

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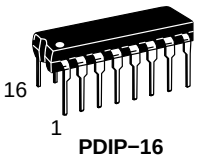
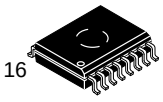
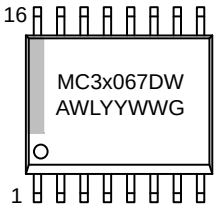
**MARKING DIAGRAMS**



**PDIP−16**
**P SUFFIX**
**CASE 648**

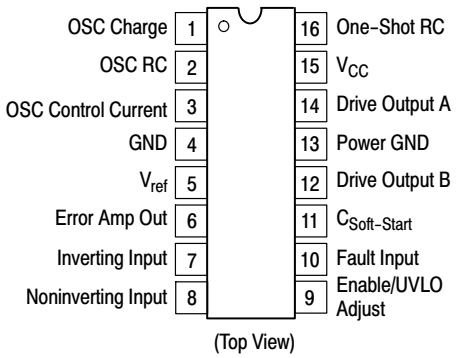



**SOIC−16W**
**DW SUFFIX**
**CASE 751G**




x = 3 or 4
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

**PIN CONNECTIONS**




(Top View)

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 20 | V |
| Drive Output Current, Source or Sink (Note 1)<br>− Continuous<br>− Pulsed (0.5 μs), 25% Duty Cycle | $I_O$ | <br>0.3<br>1.5 | A |
| Error Amplifier, Fault, One−Shot, Oscillator and Soft−Start Inputs | $V_{in}$ | − 1.0 to + 6.0 | V |
| UVLO Adjust Input | $V_{in(UVLO)}$ | − 1.0 to $V_{CC}$ | V |
| Power Dissipation and Thermal Characteristics<br>DW Suffix, Plastic Package, Case 751G<br>$T_A$ = 25°C<br>Thermal Resistance, Junction−to−Air<br>P Suffix, Plastic Package, Case 648<br>$T_A$ = 25°C<br>Thermal Resistance, Junction−to−Air | <br><br>$P_D$<br>$R_{\theta JA}$<br><br>$P_D$<br>$R_{\theta JA}$ | <br><br>862<br>145<br><br>1.25<br>100 | <br><br>mW<br>°C/W<br><br>W<br>°C/W |
| Operating Junction Temperature | $T_J$ | + 150 | °C |
| Operating Ambient Temperature<br>MC34067<br>MC33067, NCV33067 | $T_A$ | <br>0 to + 70<br>− 40 to + 85 | °C |
| Storage Temperature | $T_{stg}$ | − 55 to + 150 | °C |
| ESD Capability, HBM Model per JEDEC JESD22−A114F | − | 2.0 | kV |
| ESD Capability, CDM Model per JEDEC JESD22−C101E | − | 1.0 | kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC33067DWG | SOIC−16W<br>(Pb−Free) | 47 Units / Rail |
| MC33067DWR2G | SOIC−16W<br>(Pb−Free) | 1000 / Tape & Reel |
| NCV33067DWR2G* | SOIC−16W<br>(Pb−Free) | 1000 / Tape & Reel |
| MC33067PG | PDIP−16<br>(Pb−Free) | 25 Units / Rail |
| MC34067DWG | SOIC−16W<br>(Pb−Free) | 47 Units / Rail |
| MC34067DWR2G | SOIC−16W<br>(Pb−Free) | 1000 / Tape & Reel |
| MC34067PG | PDIP−16<br>(Pb−Free) | 25 Units / Rail |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 12 V [Note 2], $R_{OSC}$= 18.2 k, $R_{VFO}$ = 2940 Ω, $C_{OSC}$ = 300 pF, $R_T$ = 2370 Ω, $C_T$ = 300 pF, $C_L$ = 1.0 nF. For typical values $T_A$ = 25°C, for min/max values $T_A$ is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **REFERENCE SECTION** | | | | | |
| Reference Output Voltage ($I_O$ = 0 mA, $T_J$ = 25°C) | $V_{ref}$ | 5.0 | 5.1 | 5.2 | V |
| Line Regulation ($V_{CC}$ = 10 V to 18 V) | $Reg_{line}$ | − | 1.0 | 20 | mV |
| Load Regulation ($I_O$ = 0 mA to 10 mA) | $Reg_{load}$ | − | 1.0 | 20 | mV |
| Total Output Variation Over Line, Load, and Temperature | $V_{ref}$ | 4.9 | − | 5.3 | V |
| Output Short Circuit Current<br>(0°C to 70°C)<br>(−40°C to 85°C) | $I_O$ | <br>30<br>25 | <br>100<br>100 | <br>190<br>225 | mA |
| Reference Undervoltage Lockout Threshold | $V_{th}$ | 3.8 | 4.3 | 4.8 | V |
| **ERROR AMPLIFIER** | | | | | |
| Input Offset Voltage ($V_{CM}$ = 1.5 V) | $V_{IO}$ | − | 1.0 | 10 | mV |
| Input Bias Current ($V_{CM}$ = 1.5 V) | $I_{IB}$ | − | 0.2 | 1.0 | μA |
| Input Offset Current ($V_{CM}$ = 1.5 V) | $I_{IO}$ | − | 0 | 0.5 | μA |
| Open Loop Voltage Gain ($V_{CM}$ = 1.5 V, $V_O$ = 2.0 V) | $A_{VOL}$ | 70 | 100 | − | dB |
| Gain Bandwidth Product (f = 100 kHz)<br>$T_A$ = 25°C<br>$T_A$ = $T_{low}$ to $T_{high}$ | GBW | <br>3.0<br>2.7 | <br>5.0<br>− | <br>−<br>− | MHz |
| Input Common Mode Rejection Ratio ($V_{CM}$ = 1.5 V to 5.0 V) | CMR | 70 | 95 | − | dB |
| Power Supply Rejection Ratio ($V_{CC}$ = 10 V to 18 V, f = 120 Hz) | PSR | 80 | 100 | − | dB |
| Output Voltage Swing<br>High State ($I_{source}$ = 2.0 mA)<br>Low State ($I_{sink}$ = 4.0 mA) | <br>$V_{OH}$<br>$V_{OL}$ | <br>2.8<br>− | <br>3.2<br>0.6 | <br>−<br>0.8 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Maximum package power dissipation limits must be observed.
2. Adjust $V_{CC}$ above the Startup Threshold voltage before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
4. $T_{low}$ = 0°C for MC34067
   = − 40°C for MC33067, NCV33067
   $T_{high}$ = + 70°C for MC34067
   = + 85°C for MC33067, NCV33067

**ELECTRICAL CHARACTERISTICS (continued)** ($V_{CC}$ = 12 V [Note 6], $R_{OSC}$= 18.2 k, $R_{VFO}$ = 2940 Ω, $C_{OSC}$ = 300 pF, $R_T$ = 2370 Ω, $C_T$ = 300 pF, $C_L$ = 1.0 nF. For typical values $T_A$ = 25°C, for min/max values $T_A$ is the operating ambient temperature range that applies (Note 7), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | |
| Frequency (Error Amp Output Low)<br>Total Variation ($V_{CC}$ = 10 V to 18 V, $T_A$ = $T_{Low}$ to $T_{High}$) | $f_{OSC(low)}$ | 490 | 525 | 550 | kHz |
| Frequency (Error Amp Output High)<br>Total Variation ($V_{CC}$ = 10 V to 18 V, $T_A$ = $T_{Low}$ to $T_{High}$) | $f_{OSC(high)}$ | 1850 | 2050 | 2200 | kHz |
| Oscillator Control Input Voltage, Pin 3 | $V_{in}$ | – | 2.5 | – | V |
| **ONE−SHOT** | | | | | |
| Drive Output Off−Time<br>$T_A$ = 25°C<br>Total Variation ($V_{CC}$ = 10 V to 18 V, $T_A$ = $T_{Low}$ to $T_{High}$) | $t_{Blank}$ | <br>235<br>225 | <br>250<br>– | <br>270<br>280 | ns |
| **DRIVE OUTPUTS** | | | | | |
| Output Voltage<br>Low State ($I_{Sink}$ = 20 mA)<br>($I_{Sink}$ = 200 mA)<br>High State ($I_{Source}$ = 20 mA)<br>($I_{Source}$ = 200 mA) | <br>$V_{OL}$<br><br>$V_{OH}$<br> | <br>–<br>–<br>9.5<br>9.0 | <br>0.8<br>1.5<br>10.3<br>9.7 | <br>1.2<br>2.0<br>–<br>– | V |
| Output Voltage with UVLO Activated ($V_{CC}$ = 6.0 V, $I_{Sink}$ = 1.0 mA) | $V_{OL(UVLO)}$ | – | 0.8 | 1.2 | V |
| Output Voltage Rise Time ($C_L$ = 1.0 nF) | $t_r$ | – | 20 | 50 | ns |
| Output Voltage Fall Time ($C_L$ = 1.0 nF) | $t_f$ | – | 15 | 50 | ns |
| **FAULT COMPARATOR** | | | | | |
| Input Threshold | $V_{th}$ | 0.93 | 1.0 | 1.07 | V |
| Input Bias Current ($V_{Pin\ 10}$ = 0 V) | $I_{IB}$ | – | − 2.0 | − 10 | μA |
| Propagation Delay to Drive Outputs (100 mV Overdrive) | $t_{PLH(In/Out)}$ | – | 60 | 100 | ns |
| **SOFT−START** | | | | | |
| Capacitor Charge Current ($V_{Pin\ 11}$ = 2.5 V) | $I_{chg}$ | 4.5 | 9.0 | 14 | μA |
| Capacitor Discharge Current ($V_{Pin\ 11}$ = 2.5 V) | $I_{dischg}$ | 3.0 | 8.0 | – | mA |
| **UNDERVOLTAGE LOCKOUT** | | | | | |
| Startup Threshold, $V_{CC}$ Increasing<br>Enable/UVLO Adjust Pin Open<br>Enable/UVLO Adjust Pin Connected to $V_{CC}$ | $V_{th(UVLO)}$ | <br>14.8<br>8.0 | <br>16<br>9.0 | <br>17.2<br>10 | V |
| Minimum Operating Voltage After Turn−On, $V_{CC}$ Decreasing<br>Enable/UVLO Adjust Pin Open<br>Enable/UVLO Adjust Pin Connected to $V_{CC}$ | $V_{CC(min)}$ | <br>8.0<br>7.6 | <br>9.0<br>8.6 | <br>10<br>9.6 | V |
| Enable/UVLO Adjust Shutdown Threshold Voltage | $V_{th(Enable)}$ | 6.0 | 7.0 | – | V |
| Enable/UVLO Adjust Input Current (Pin 9 = 0 V) | $I_{in(Enable)}$ | – | − 0.2 | − 1.0 | mA |
| **TOTAL DEVICE** | | | | | |
| Power Supply Current (Enable/UVLO Adjust Pin Open)<br>Startup ($V_{CC}$ = 13.5 V)<br>Operating ($f_{OSC}$ = 500 kHz) (Note 6) | $I_{CC}$ | <br>–<br>– | <br>0.5<br>27 | <br>0.8<br>35 | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Maximum package power dissipation limits must be observed.
6. Adjust $V_{CC}$ above the Startup Threshold voltage before setting to 12 V.
7. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
8. $T_{low}$ = 0°C for MC34067
   = − 40°C for MC33067, NCV33067
   $T_{high}$ = + 70°C for MC34067
   = + 85°C for MC33067, NCV33067

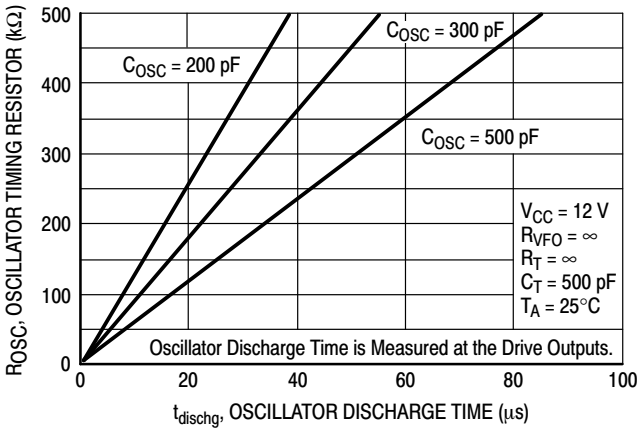



**Figure 2. Oscillator Timing Resistor versus Discharge Time**

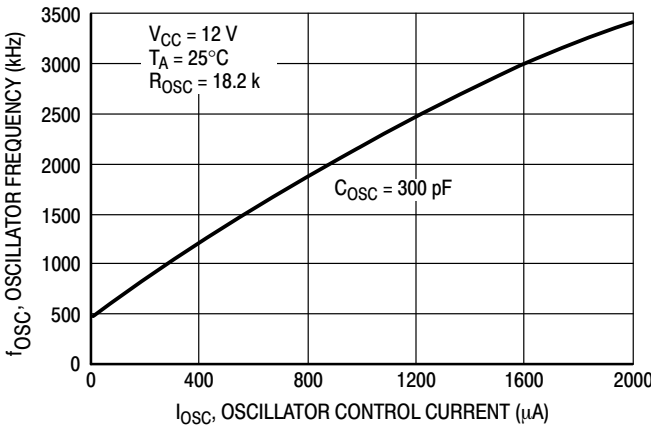



**Figure 3. Oscillator Frequency versus Oscillator Control Current**

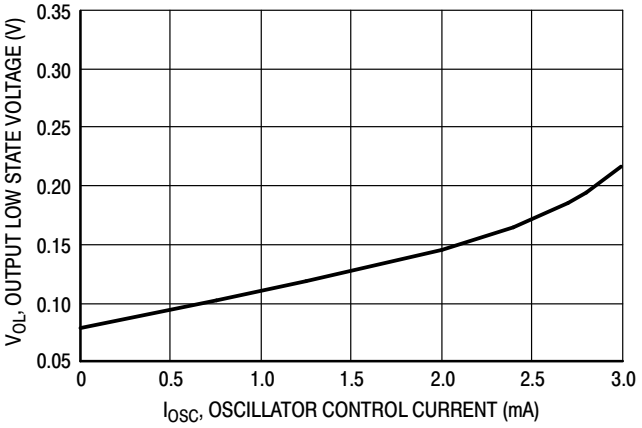



**Figure 4. Error Amp Output Low State Voltage versus Oscillator Control Current**

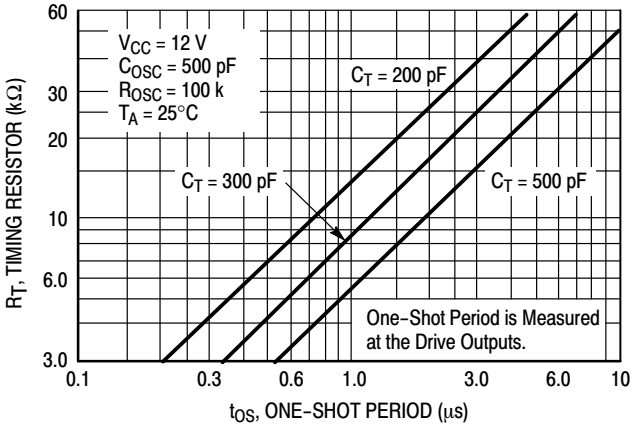



**Figure 5. One−Shot Timing Resistor versus Period**

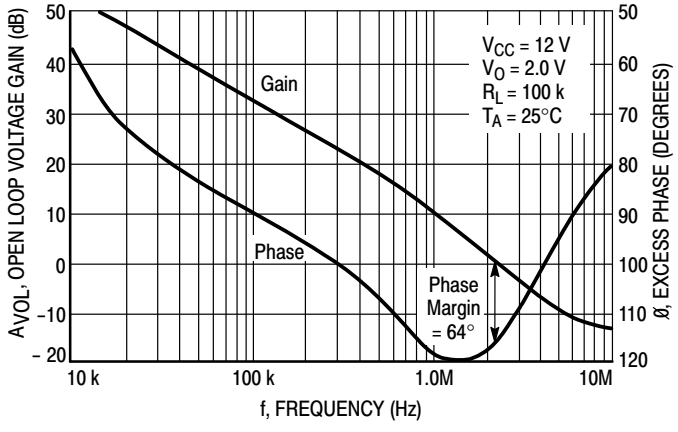



**Figure 6. Open Loop Voltage Gain and Phase versus Frequency**

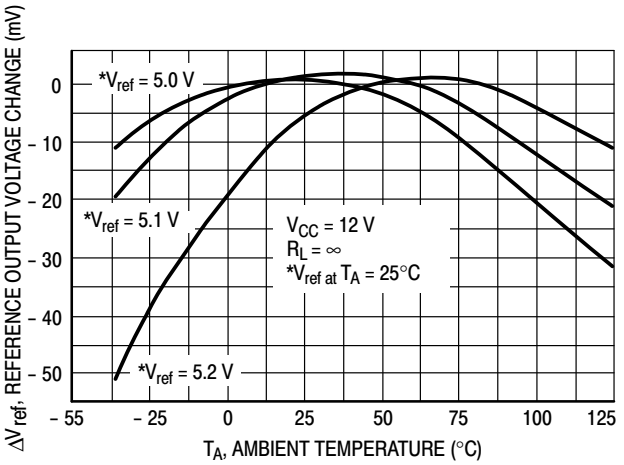



**Figure 7. Reference Output Voltage Change versus Temperature**

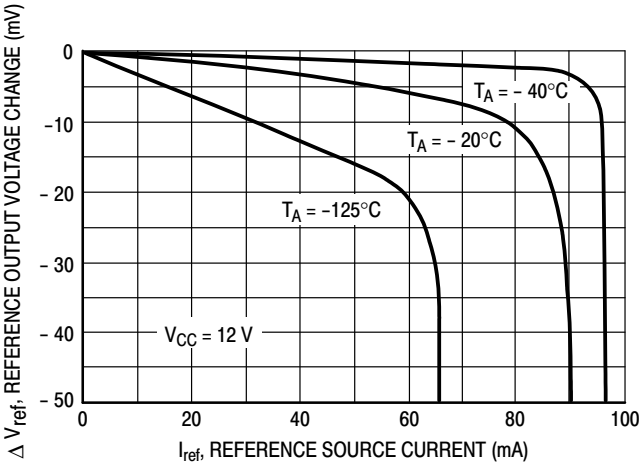



**Figure 8. Reference Output Voltage Change versus Source Current**

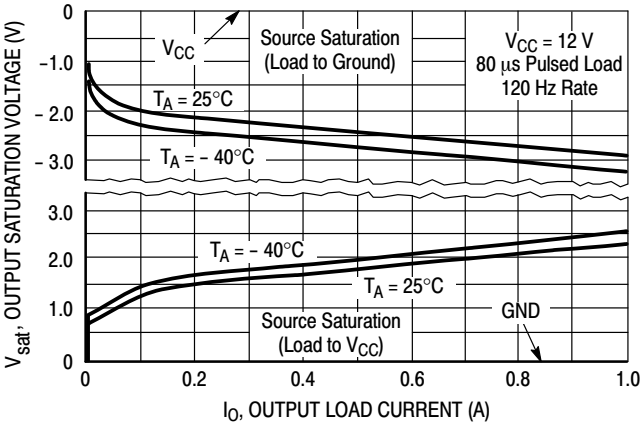



**Figure 9. Drive Output Saturation Voltage versus Load Current**

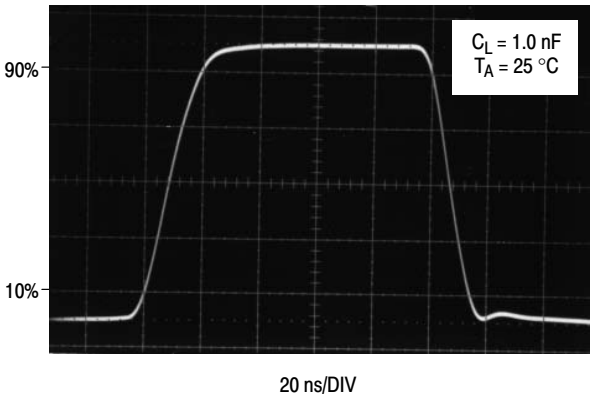



**Figure 10. Drive Output Waveform**

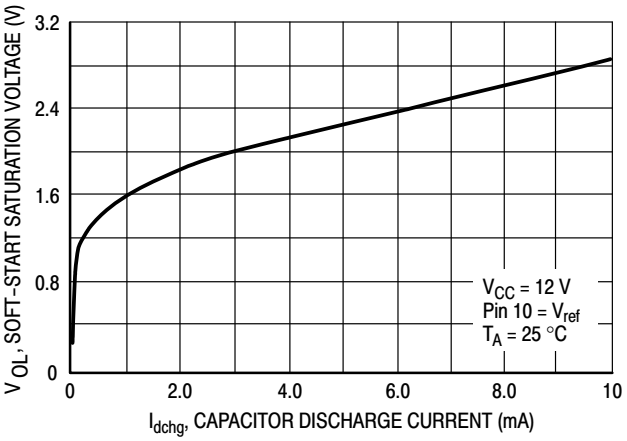



**Figure 11. Soft−Start Saturation Voltage versus Capacitor Discharge Current**

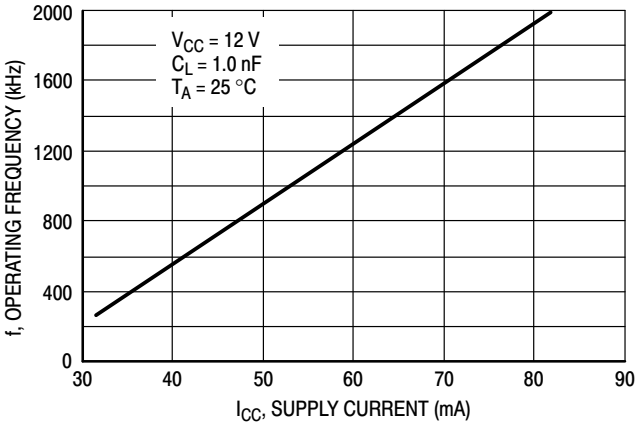



**Figure 12. Operating Frequency versus Supply Current**

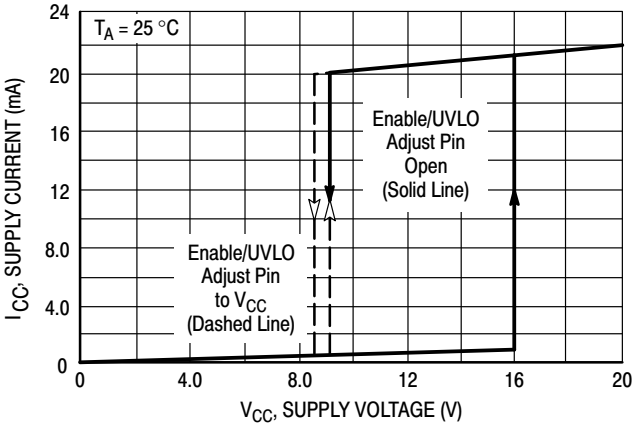



**Figure 13. Supply Current versus Supply Voltage**

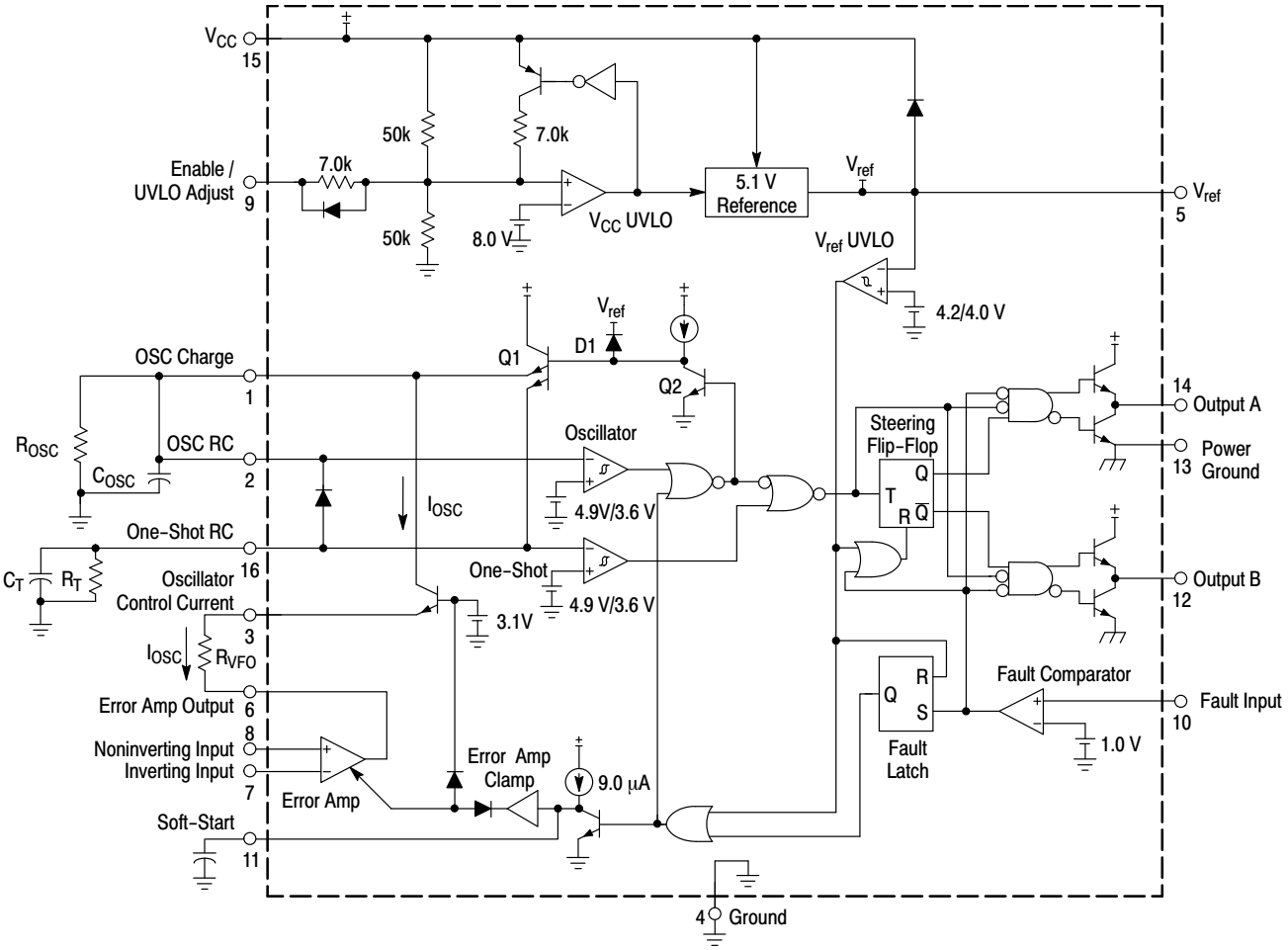
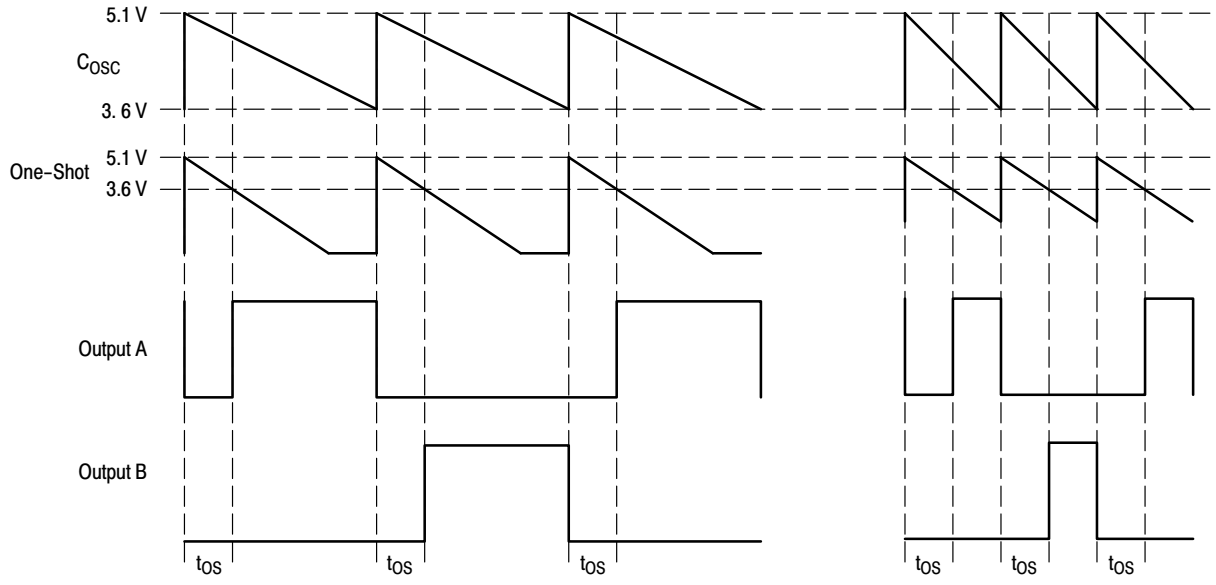



**Figure 14. MC34067 Representative Block Diagram**




High State Error Amp output, minimum $I_{OSC}$ current occurring at minimum input voltage, maximum load.

Low State Error Amp output, maximum $I_{OSC}$ current occurring at maximum input voltage, minimum load.

**Figure 15. Timing Diagram**

## OPERATING DESCRIPTION

### Introduction

As power supply designers have strived to increase power conversion efficiency and reduce passive component size, high frequency resonant mode power converters have emerged as attractive alternatives to conventional pulse−width modulated control. When compared to pulse−width modulated converters, resonant mode control offers several benefits including lower switching losses, higher efficiency, lower EMI emission, and smaller size. A new integrated circuit has been developed to support this trend in power supply design. The MC34067 Resonant Mode Controller is a high performance bipolar IC dedicated to variable frequency power control at frequencies exceeding 1.0 MHz. This integrated circuit provides the features and performance specifically for zero voltage switching resonant mode power supply applications.

The primary purpose of the control chip is to provide a fixed off−time to the gates of external power MOSFETs at a repetition rate regulated by a feedback control loop. Additional features of the IC ensure that system startup and fault conditions are administered in a safe, controlled manner.

A simplified block diagram of the IC is shown on the front page, which identifies the main functional blocks and the block−to−block interconnects. Figure 14 is a detailed functional diagram which accurately represents the internal circuitry. The various functions can be divided into two sections. The first section includes the primary control path which produces precise output pulses at the desired frequency. Included in this section are a variable frequency Oscillator, a One−Shot, a pulse Steering Flip−Flop, a pair of power MOSFET Drivers, and a wide bandwidth Error Amplifier. The second section provides several peripheral support functions including a voltage reference, undervoltage lockout, soft−start circuit, and a fault detector.

### Primary Control Path

The output pulse width and repetition rate are regulated through the interaction of the variable frequency Oscillator, One−Shot timer and Error Amplifier. The Oscillator triggers the One−Shot which generates a pulse that is alternately steered to a pair of totem pole output drivers by a toggle Flip−Flop. The Error Amplifier monitors the output of the regulator and modulates the frequency of the Oscillator. High speed Schottky logic is used throughout the primary control channel to minimize delays and enhance high frequency characteristics.

### Oscillator

The characteristics of the variable frequency Oscillator are crucial for precise controller performance at high operating frequencies. In addition to triggering the One−Shot timer and initiating the output deadtime, the oscillator also determines the initial voltage for the one−shot capacitor. The Oscillator is designed to operate at frequencies exceeding 1.0 MHz. The Error Amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily and accurately programmed by the proper selection of external components.

The functional diagram of the Oscillator and One−Shot timer is shown in Figure 16. The oscillator capacitor ($C_{OSC}$) is initially charged by transistor Q1. When $C_{OSC}$ exceeds the 4.9 V upper threshold of the oscillator comparator, the base of Q1 is pulled low allowing $C_{OSC}$ to discharge through the external resistor, ($R_{OSC}$), and the oscillator control current, ($I_{OSC}$). When the voltage on $C_{OSC}$ falls below the 3.6 V lower threshold of the comparator, Q1 turns on and again charges $C_{OSC}$.

$C_{OSC}$ charges from 3.6 V to 5.1 V in less than 50 ns. The high slew rate of $C_{OSC}$ and the propagation delay of the comparator make it difficult to control the peak voltage. This accuracy issue is overcome by clamping the base of Q1 through a diode to a voltage reference. The peak voltage of the oscillator waveform is thereby precisely set at 5.1 V.

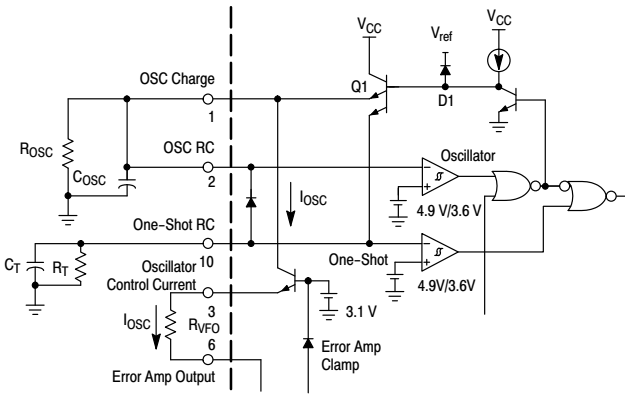



**Figure 16. Oscillator and One−Shot Timer**

The frequency of the Oscillator is modulated by varying the current flowing out of the Oscillator Control Current ($I_{OSC}$) pin. The $I_{OSC}$ pin is the output of a voltage regulator. The input of the voltage regulator is tied to the variable frequency oscillator. The discharge current of the Oscillator increases by increasing the current out of the $I_{OSC}$ pin. Resistor $R_{VFO}$ is used in conjunction with the Error Amp output to change the $I_{OSC}$ current. Maximum frequency occurs when the Error Amplifier output is at its low state with a saturation voltage of 0.1 V at 1.0 mA.

The minimum oscillator frequency will result when the $I_{OSC}$ current is zero, and $C_{OSC}$ is discharged through the external resistor ($R_{OSC}$). This occurs when the Error Amplifier output is at its high state of 2.5 V. The minimum and maximum oscillator frequencies are programmed by the proper selection of resistor $R_{OSC}$ and $R_{VFO}$.

The minimum frequency is programmed by $R_{OSC}$ using Equation 1:

$$R_{OSC} = \frac{\frac{1}{f_{(min)}} - t_{PD}}{C_{OSC}\,\ell n\left(\frac{5.1}{3.6}\right)} = \frac{t_{(max)} - 70\ ns}{0.348\,C_{OSC}} \quad \text{(eq. 1)}$$

where $t_{PD}$ is the internal propagation delay.

The maximum oscillator frequency is set by the current through resistor $R_{VFO}$. The current required to discharge $C_{OSC}$ at the maximum oscillator frequency can be calculated by Equation 2:

$$I_{(max)} = C_{OSC}\frac{5.1 - 3.6}{\frac{1}{f_{(max)}}} = 1.5 C_{OSC} f_{(max)} \quad \text{(eq. 2)}$$

The discharge current through $R_{OSC}$ must also be known and can be calculated by Equation 3:

$$I_{R_{OSC}} = \frac{5.1 - 3.6}{R_{OSC}}\,\varepsilon^{\left(-\frac{\frac{1}{f_{(min)}}}{R_{OSC}C_{OSC}}\right)} = \frac{1.5}{R_{OSC}}\,\varepsilon^{\left(-\frac{1}{f_{(min)}R_{OSC}C_{OSC}}\right)} \quad \text{(eq. 3)}$$

Resistor $R_{VFO}$ can now be calculated by Equation 4:

$$R_{VFO} = \frac{2.5 - V_{EAsat}}{I_{(max)} - I_{R_{OSC}}} \quad \text{(eq. 4)}$$

### One−Shot Timer

The One−Shot is designed to disable both outputs simultaneously providing a deadtime before either output is enabled. The One−Shot capacitor ($C_T$) is charged concurrently with the oscillator capacitor by transistor Q1, as shown in Figure 16. The one−shot period begins when the oscillator comparator turns off Q1, allowing $C_T$ to discharge. The period ends when resistor $R_T$ discharges $C_T$ to the threshold of the One−Shot comparator. The lower threshold of the One−Shot is 3.6 V. By choosing $C_T$, $R_T$ can by solved by Equation 5:

$$R_T = \frac{t_{OS}}{C_T\,\ell n\left(\frac{5.1}{3.6}\right)} = \frac{t_{OS}}{0.348\,C_T} \quad \text{(eq. 5)}$$

Errors in the threshold voltage and propagation delays through the output drivers will affect the One−Shot period. To guarantee accuracy, the output pulse of the control chip is trimmed to within 5% of 250 ns with nominal values of $R_T$ and $C_T$.

The outputs of the Oscillator and One−Shot comparators are OR'd together to produce the pulse $t_{OS}$, which drives the Flip−Flop and output drivers. The output pulse ($t_{OS}$) is initiated by the Oscillator and terminated by the One−Shot comparator. With zero voltage resonant mode converters, the oscillator discharge time should never be set less than the one−shot period.

### Error Amplifier

A fully accessible high performance Error Amplifier is provided for feedback control of the power supply system. The Error Amplifier is internally compensated and features dc open loop gain greater than 70 dB, input offset voltage of less than 10 mV and a guaranteed minimum gain−bandwidth product of 2.5 MHz. The input common mode range extends from 1.5 V to 5.1 V, which includes the reference voltage.

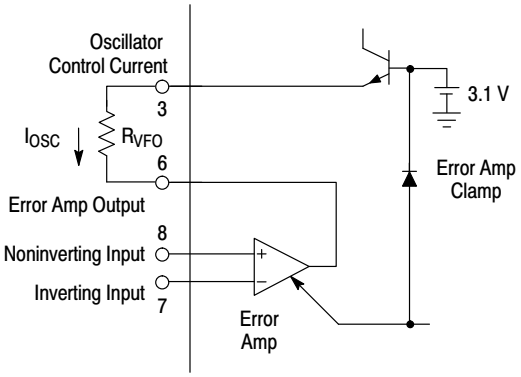



**Figure 17. Error Amplifier and Clamp**

When the Error Amplifier output is coupled to the $I_{OSC}$ pin by $R_{VFO}$, as illustrated in Figure 17, it provides the Oscillator Control Current, $I_{OSC}$. The output swing of the Error Amplifier is restricted by a clamp circuit to improve its transient recovery time.

### Output Section

The pulse($t_{OS}$), generated by the Oscillator and One−Shot timer is gated to dual totem−pole output drives by the Steering Flip−Flop shown in Figure 18. Positive transitions of $t_{OS}$ toggle the Flip−Flop, which causes the pulses to alternate between Output A and Output B. The flip−flop is reset by the undervoltage lockout circuit during startup to guarantee that the first pulse appears at Output A.

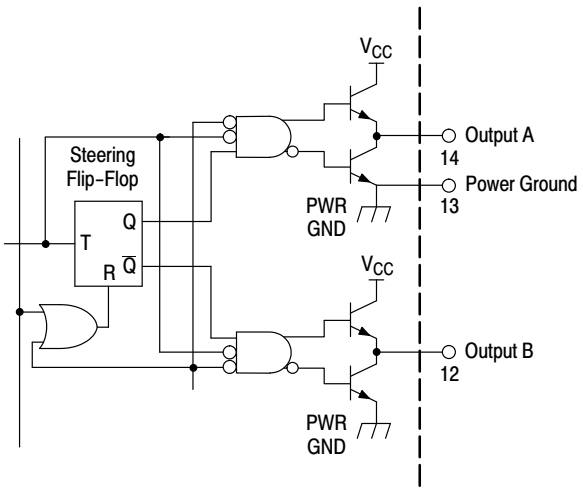



**Figure 18. Steering Flip−Flop and Output Drivers**

The totem−pole output drivers are ideally suited for driving power MOSFETs and are capable of sourcing and sinking 1.5 A. Rise and fall times are typically 20 ns and 15 ns respectfully when driving a 1.0 nF load. High source/sink capability in a totem−pole driver normally increases the risk of high cross conduction current during output transitions. The MC34067 utilizes a unique design that virtually eliminates cross conduction, thus controlling the chip power dissipation at high frequencies. A separate power ground pin is provided to isolate the sensitive analog circuitry from large transient currents.

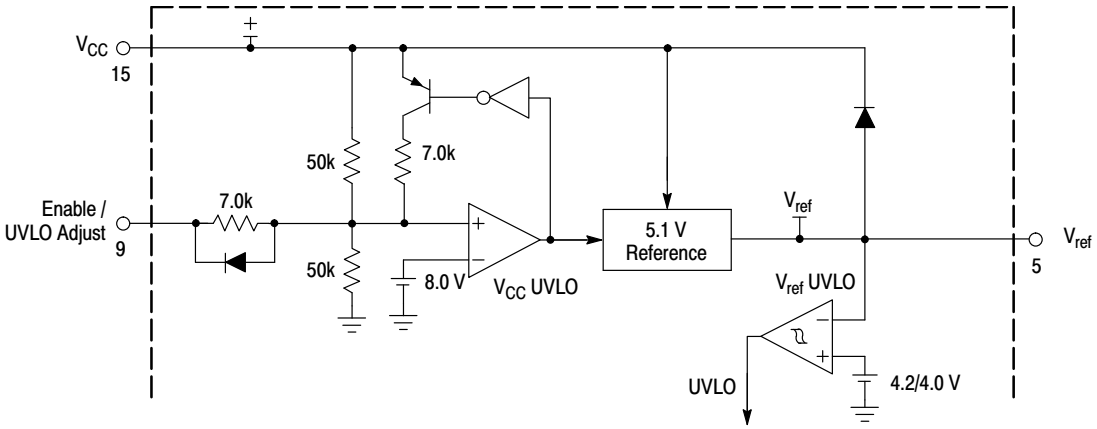



**Figure 19. Undervoltage Lockout and Reference**

## PERIPHERAL SUPPORT FUNCTIONS

The MC34067 Resonant Controller provides a number of support and protection functions including a precision voltage reference, undervoltage lockout comparators, soft−start circuitry, and a fault detector. These peripheral circuits ensure that the power supply can be turned on and off in a controlled manner and that the system will be quickly disabled when a fault condition occurs.

### Undervoltage Lockout and Voltage Reference

Separate undervoltage lockout comparators sense the input $V_{CC}$ voltage and the regulated reference voltage as illustrated in Figure 19. When $V_{CC}$ increases to the upper threshold voltage, the $V_{CC}$ UVLO comparator enables the Reference Regulator. After the $V_{ref}$ output of the Reference Regulator rises to 4.2 V, the $V_{ref}$ UVLO comparator switches the UVLO signal to a logic zero state enabling the primary control path. Reducing $V_{CC}$ to the lower threshold voltage causes the $V_{CC}$ UVLO comparator to disable the Reference Regulator. The $V_{ref}$ UVLO comparator then switches the UVLO output to a logic one state disabling the controller.

The Enable/UVLO Adjust pin allows the power supply designer to select the $V_{CC}$ UVLO threshold voltages. When this pin is open, the comparator switches the controller on at 16 V and off at 9.0 V. If this pin is connected to the $V_{CC}$ terminal, the upper and lower thresholds are reduced to 9.0 V and 8.6 V, respectively. Forcing the Enable/UVLO Adjust pin low will pull the $V_{CC}$ UVLO comparator input low (through an internal diode) turning off the controller.

The Reference Regulator provides a precise 5.1 V reference to internal circuitry and can deliver up to 10 mA to external loads. The reference is trimmed to better than 2% initial accuracy and includes active short circuit protection.

### Fault Detection

Converter protection from adverse operating conditions can be implemented with proper use of the Fault Comparator and Latch blocks that are illustrated in Figure 20. The Fault Comparator has an input threshold of 1.0 V and when exceeded, sets the Fault Latch and generates two logic signals that simultaneously disable the primary control path. The signal line labeled “Fault” connects directly to two gates that control the output drivers. This direct path reduces the driver turn−off propagation delay to approximately 70 ns. The Fault Latch output is OR’ed with the UVLO output that is derived from the $V_{ref}$ UVLO comparator, to produce the logic output labeled “UVLO+Fault”. This signal disables the Oscillator and the One−Shot by forcing both the $C_{OSC}$ and $C_T$ capacitors to be continually charged.

The Fault Latch is automatically reset during startup by a logic “1” that appears at the $V_{ref}$ UVLO comparator output. The latch can also be reset after startup by momentarily pulling the Enable/UVLO Adjust pin low to disable the Reference. Note that after activation, the Fault Latch will remain in a set state only as long as $V_{CC}$ is provided to the MC34067. Also, Drive Output B will assume a high state if the Fault input signal drops below the 1.0 V threshold level even after the Fault Latch has been set. In some applications this characteristic could be problematic but it can be easily remedied by AC coupling Drive Output B.

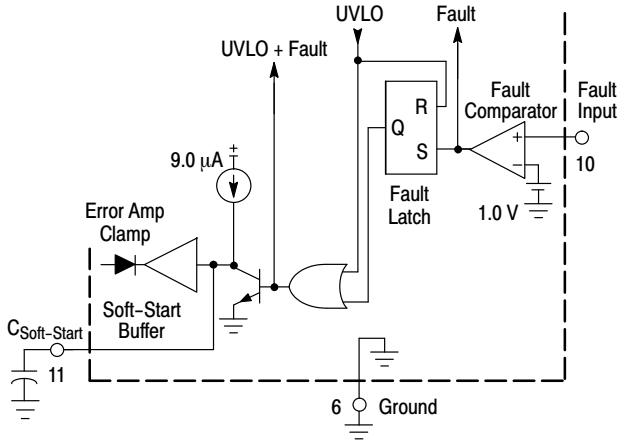



**Figure 20. Fault Detector and Soft−Start**

### Soft−Start Circuit

The Soft−Start circuit shown in Figure 20 forces the variable frequency Oscillator to start at the maximum frequency and ramp downward until regulated by the feedback control loop. The external capacitor at the $C_{Soft-Start}$ terminal is initially discharged by the UVLO+Fault signal. The low voltage on the capacitor passes through the Soft−Start Buffer to hold the Error Amplifier output low. After UVLO+Fault switches to a logic zero, the soft−start capacitor is charged by a 9.0 μA current source. The buffer allows the Error Amplifier output to follow the soft−start capacitor until it is regulated by the Error Amplifier inputs. The soft−start function is generally applicable to controllers operating below resonance and can be disabled by simply opening the $C_{Soft-Start}$ terminal.

## APPLICATIONS INFORMATION

The MC34067 is specifically designed for zero voltage switching (ZVS) quasi−resonant converter (QRC) applications. The IC is optimized for double−ended push−pull or bridge type converters operating in continuous conduction mode. Operation of this type of ZVS with resonant properties is similar to standard push−pull or bridge circuits in that the energy is transferred during the transistor on−time. The difference is that a series resonant tank is usually introduced to shape the voltage across the power transistor prior to turn−on. The resonant tank in this topology is not used to deliver energy to the output as is the case with zero current switch topologies. When the power transistor is enabled the voltage across it should already be zero, yielding minimal switching loss. Figure 21 shows a timing diagram for a half−bridge ZVS QRC. An application circuit is shown in Figure 22. The circuit built is a dc to dc half−bridge converter delivering 75 W to the output from a 48 V source.

When building a zero voltage switch (ZVS) circuit, the objective is to waveshape the power transistor's voltage waveform so that the voltage across the transistor is zero when the device is turned on. The purpose of the control IC is to allow a resonant tank to waveshape the voltage across the power transistor while still maintaining regulation. This is accomplished by maintaining a fixed deadtime and by varying the frequency; thus the effective duty cycle is changed.

Primary side resonance can be used with ZVS circuits. In the application circuit, the elements that make the resonant tank are the primary leakage inductance of the transformer ($L_L$) and the average output capacitance ($C_{OSS}$) of a power MOSFET ($C_R$).

The desired resonant frequency for the application circuit is calculated by Equation 6:

$$f_r = \frac{1}{2\pi\sqrt{L_L 2C_R}} \quad \text{(eq. 6)}$$

In the application circuit, the operating voltage is low and the value of $C_{OSS}$ versus Drain Voltage is known. Because the $C_{OSS}$ of a MOSFET changes with drain voltage, the value of the $C_R$ is approximated as the average $C_{OSS}$ of the MOSFET. For the application circuit the average $C_{OSS}$ can be calculated by Equation 7:

$$C_R = \sqrt{2} * C_{OSS} \text{ measured at } \frac{1}{2} V_{in} \quad \text{(eq. 7)}$$

The MOSFET chosen fixes $C_R$ and that $L_L$ is adjusted to achieve the desired resonant frequency.

However, the desired resonant frequency is less critical than the leakage inductance. Figure 21 shows the primary current ramping toward its peak value during the resonant transition. During this time, there is circulating current flowing through the secondary inductance, which effectively makes the primary inductance appear shorted. Therefore, the current through the primary will ramp to its peak value at a rate controlled by the leakage inductance and the applied voltage. Energy is not transferred to the secondary during this stage, because the primary current has not overcome the circulating current in the secondary. The larger the leakage inductance, the longer it takes for the primary current to slew. The practical effect of this is to lower the duty cycle, thus reducing the operating range.

The maximum duty cycle is controlled by the leakage inductance, not by the MC34067. The One−Shot in the MC34067 only assures that the power switch is turned on under a zero voltage condition. Adjust the one−shot period so that the output switch is activated while the primary current is slewing but before the current changes polarity. The resonant stage should then be designed to be as long as the time for the primary current to go to 0 A.

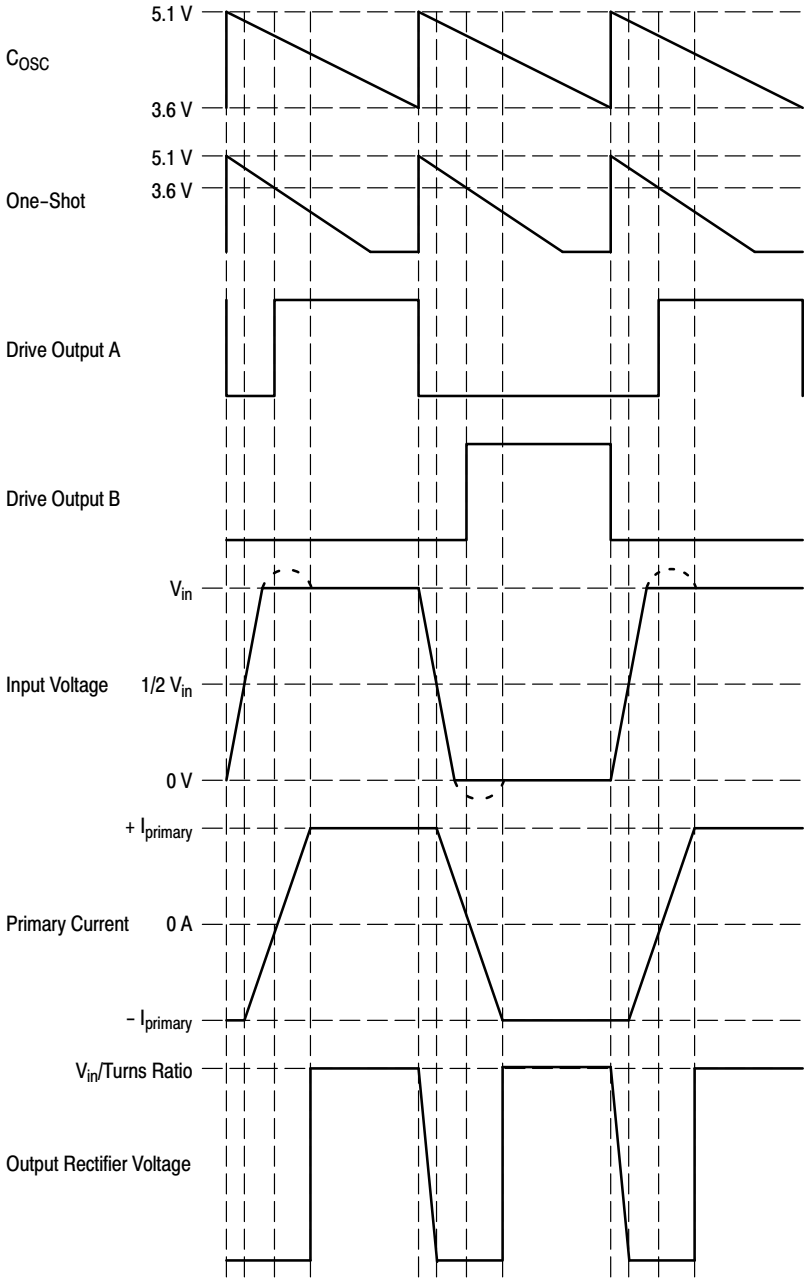
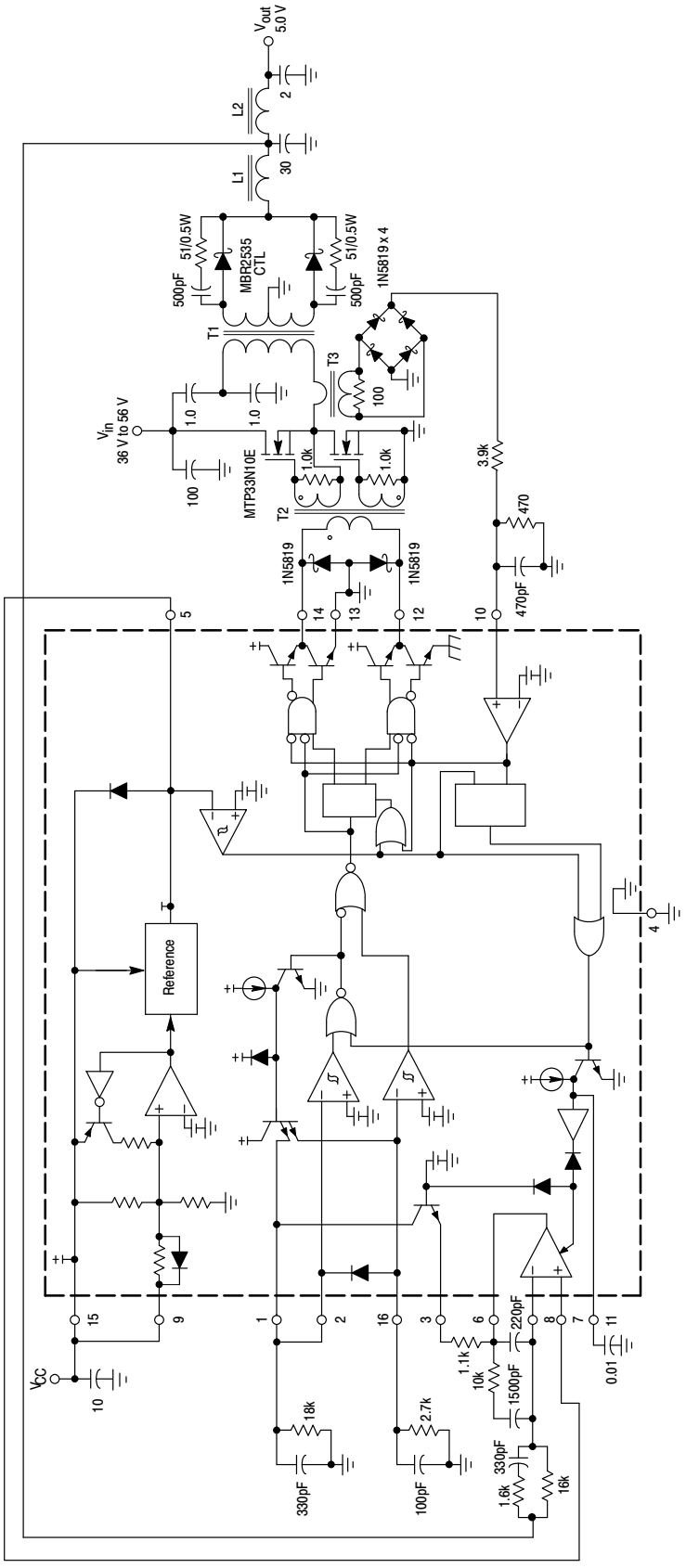



**Figure 21. Application Timing Diagram**




T1 = Primary: 12 turns #48 AWG (1300 strands litz wire)
Secondary: 6 turns center tapped #48 AWG (1300 strands litz wire)
Core: Philips 3F3 4312 020 4124
Bobbin: Philips 4322 021 3525
Primary Leakage Inductance = 1.0 μH

T2 = All windings: 8 turns #36 AWG
Core: Philips 3F3 EP7−3F3
Bobbin: Philips EP7PCB1−6

T3 = Coilcraft D1870 (100 turns)

L1 = 2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3 EP10−3F3
Bobbin: Philips EP10PCB1−8
Inductance = 1.8 μH

L2 = 5 turns #48 AWG (1300 strands litz wire)
Core: 0.5″ diameter air code
Inductance = 100 nH

Heatsinks = AAVID Engineering Inc. 533402B02552 with clip
MC34067−5803

Insulators = Berquist Sil−Pad 1500

| Test | Conditions | Results |
|---|---|---|
| Line Regulation | $V_{in}$ = 40 V to 56 V, $I_O$ =15 A | 20 mV = ±0.198% |
| Load Regulation | $V_{in}$ = 48 V, $I_O$ = 10 A to 15 A | 4.0 mV = ±0.039% |
| Output Ripple | $V_{in}$ = 48 V, $I_O$ = 15 A, $f_{switch}$ = 1.0 MHz | 25 $mV_{p-p}$ |
| Efficiency | $V_{in}$ = 48 V, $I_O$ = 10 A, $f_{switch}$ = 1.7 MHz<br>$V_{in}$ = 48 V, $I_O$ = 15 A, $f_{switch}$ = 1.0 MHz | 83.5%<br>84.2% |

**Figure 22. Application Circuit**

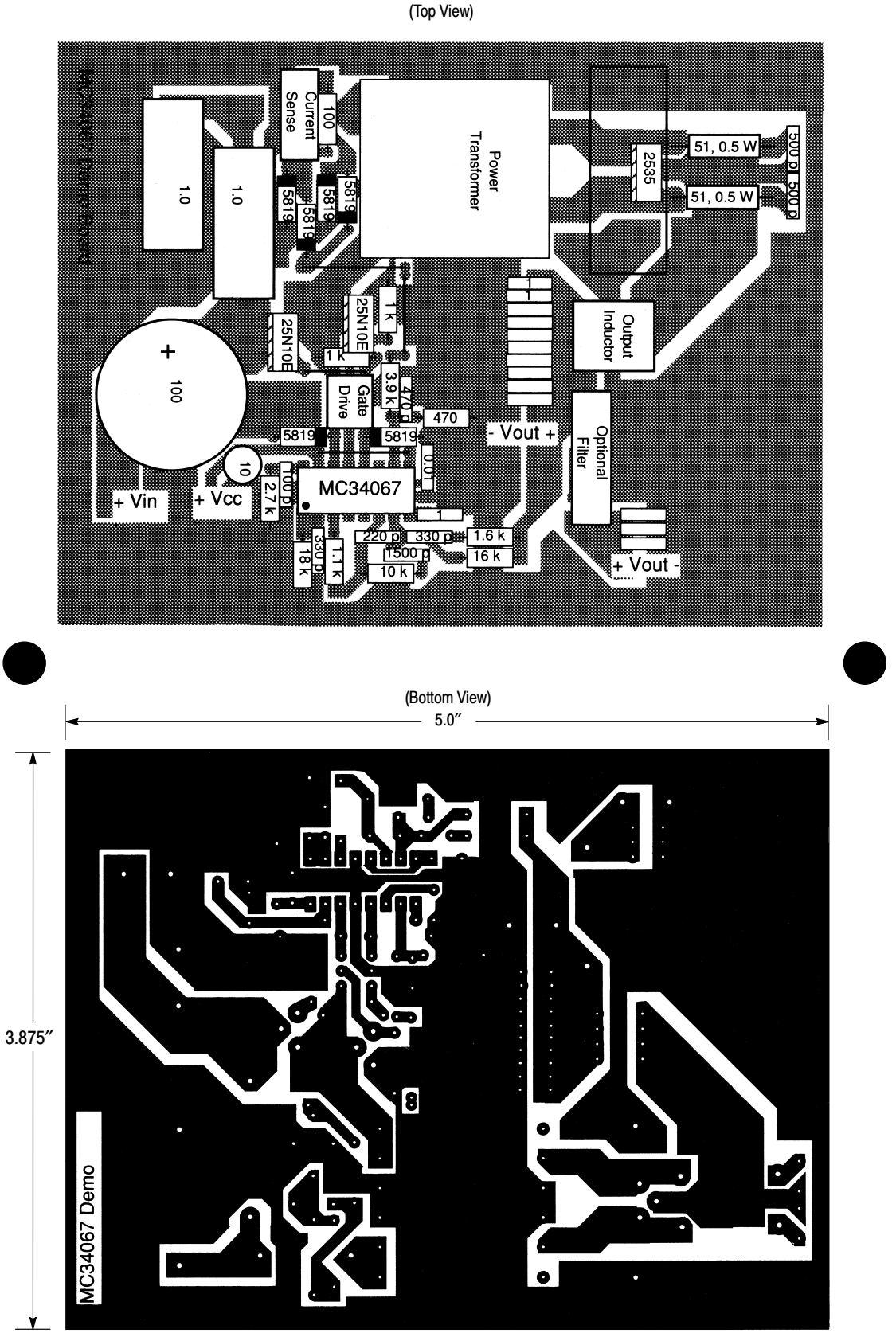


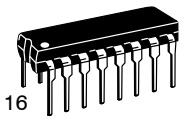

**Figure 23. Printed Circuit Board and Component Layout**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

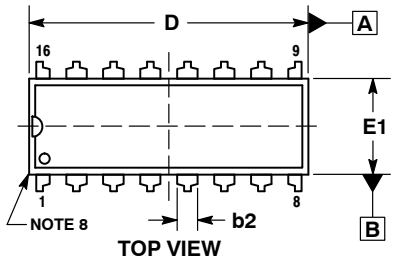
ON Semiconductor®

**PDIP−16**
CASE 648−08
ISSUE V

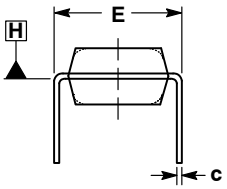
DATE 22 APR 2015



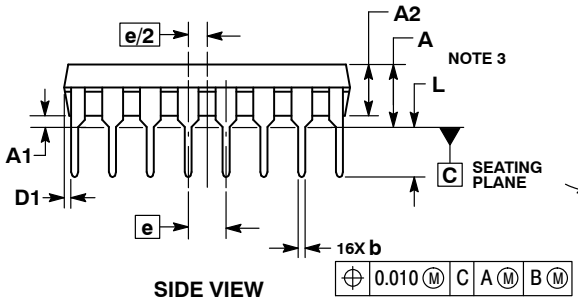

SCALE 1:1



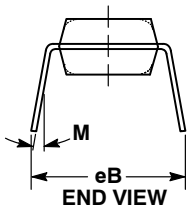

TOP VIEW




END VIEW
WITH LEADS CONSTRAINED
NOTE 5




SIDE VIEW




END VIEW
NOTE 6

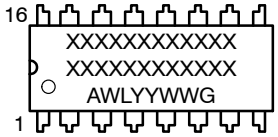
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | ---- | 0.210 | --- | 5.33 |
| A1 | 0.015 | ---- | 0.38 | --- |
| A2 | 0.115 | 0.195 | 2.92 | 4.95 |
| b | 0.014 | 0.022 | 0.35 | 0.56 |
| b2 | 0.060 TYP | | 1.52 TYP | |
| C | 0.008 | 0.014 | 0.20 | 0.36 |
| D | 0.735 | 0.775 | 18.67 | 19.69 |
| D1 | 0.005 | ---- | 0.13 | --- |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 |
| e | 0.100 BSC | | 2.54 BSC | |
| eB | ---- | 0.430 | --- | 10.92 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| M | ---- | 10° | --- | 10° |

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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# MECHANICAL CASE OUTLINE
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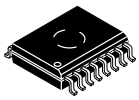
**SOIC−16 WB**
CASE 751G
ISSUE E

DATE 08 OCT 2021



1
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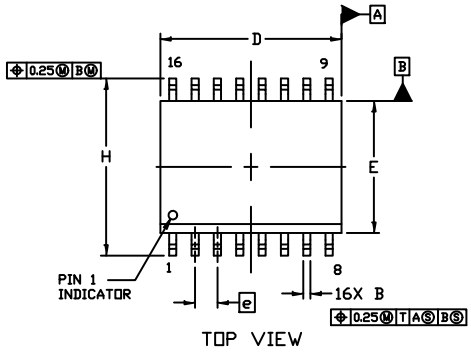
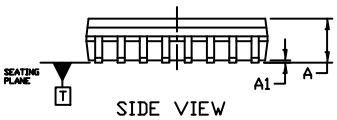
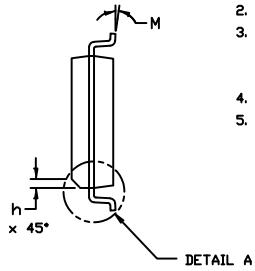


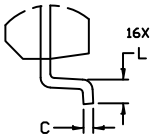

TOP VIEW




SIDE VIEW



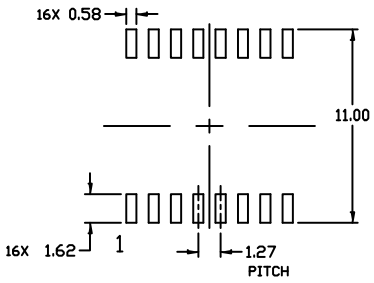

END VIEW




DETAIL A
2X SCALE

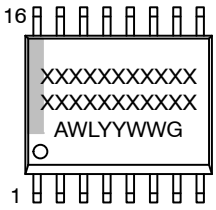
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN. | MAX. |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.53 REF | |
| L | 0.50 | 0.90 |
| M | 0° | 7° |




RECOMMENDED
MOUNTING FOOTPRINT

### GENERIC
### MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales