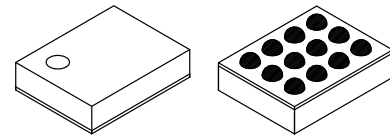


Over-Voltage Protection Load Switch

FPF2281



WLCSP12 1.288x1.828x0.586
CASE 567QX

Description

The FPF2281 features a low- R_{ON} internal FET and an operating range of 2.5 V_{DC} to 25 V_{DC} (absolute maximum of 29 V_{DC}). An internal clamp is capable of shunting surge voltages > 100 V, protecting downstream components and enhancing system robustness. The FPF2281 features over-voltage protection that powers down the internal FET if the input voltage exceeds the OVP threshold. The OVP threshold is adjustable with optional external resistors. Over-temperature protection also powers down the device at 130°C (typical). Exceptionally low off-state current (< 1 μA maximum) facilitates compliance with standby power requirements.

The FPF2281 is available in a fully “green” compliant 1.3 mm × 1.8 mm Wafer-Level Chip-Scale Package (WLCSP) with backside laminate.

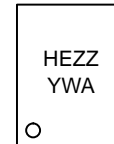
Features

- Surge Protection
 - ◆ IEC 61000-4-5: > 100 V
- Over-Voltage Protection (OVP)
- Over-Temperature Protection (OTP)
- ESD Protection
 - ◆ Human Body Model (HBM): > 3.5 kV
 - ◆ Charged Device Model (CDM): > 2 kV
 - ◆ IEC 61000-4-2 Air Discharge: > 15 kV
 - ◆ IEC 61000-4-2 Contact Discharge: > 8 kV
- This is a Pb-Free Device

Applications

- Mobile Handsets and Tablets
- Portable Media Players
- MP3 Players

MARKING DIAGRAM



- HE = Specific Device Code
- ZZ = Assembly Lot Code
- Y = Year
- W = Work Week
- A = Assembly Location

ORDERING INFORMATION

Part Number	Top Marking	Operating Temperature Range	Package	Shipping†
FPF2281BUCX-F130	HE	-40°C to 85°C	WLCSP12 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FPF2281

Block Diagram

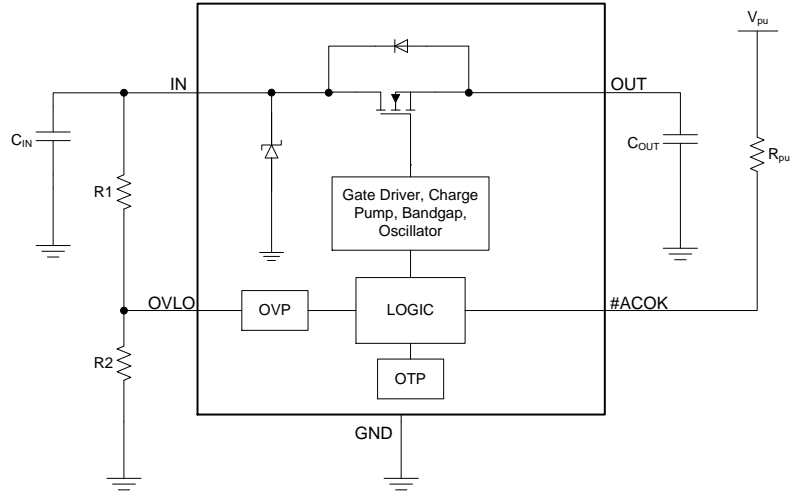


Figure 1. Functional Block Diagram

FPF2281

Pin Configuration

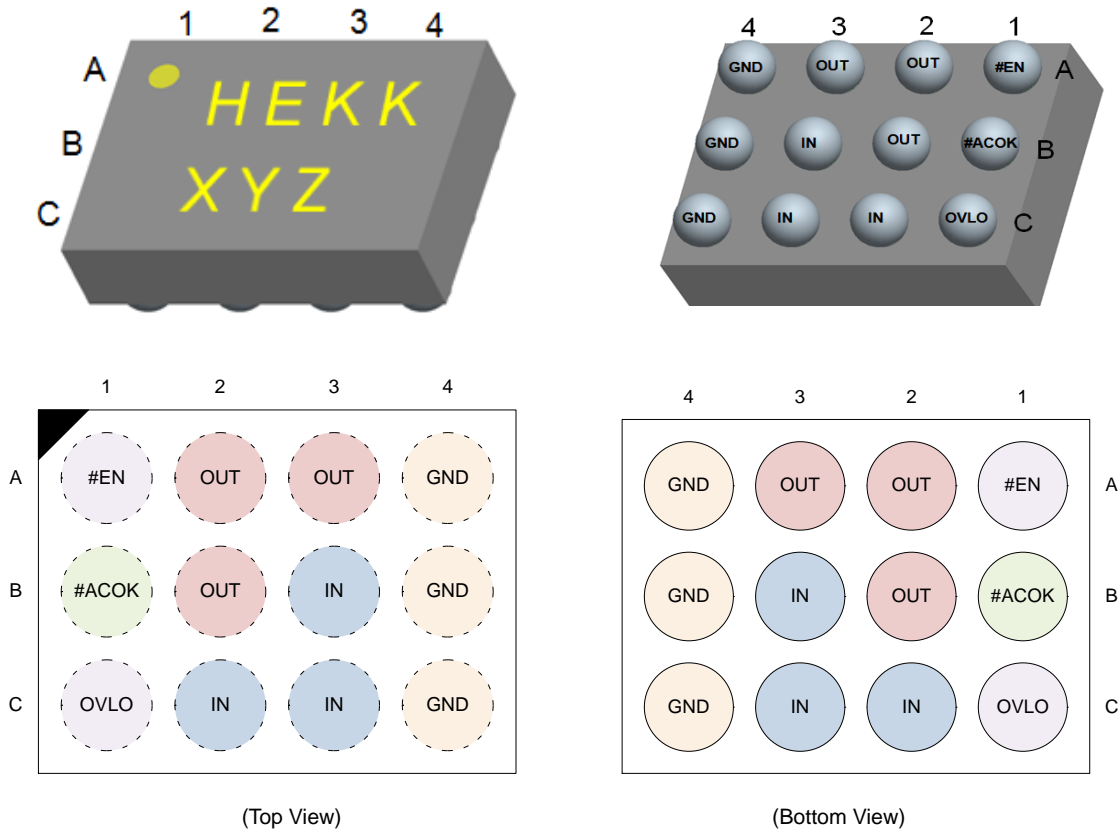


Figure 2. Pin Configuration

PIN DEFINITIONS

Name	Bump	Type	Description	
IN	B3, C2, C3	Input/Supply	Switch Input and Device Supply	
OUT	A2, A3, B2	Output	Switch Output to Load	
#ACOK	B1	Output (Open Drain)	1	$V_{IN} < V_{IN_min}$ or $V_{IN} \geq V_{OVLO}$
			0	Voltage Stable
#EN	A1	Input	Device Enable (Active LOW)	
OVLO	C1	Input	Over-Voltage Lockout Adjustment Pin	
GND	A4, B4, C4	Supply	Device Ground	

Over-Voltage Lockout (OVLO) Calculation

OVLO can be set externally and override default OVP. By connecting an external resistor-driver to the OVLO pin. Equation (1) can produce the desired trip voltage and resistor values.

$$V_{IN_OVLO} = V_{OVLO_TH} \times [1 + R1/R2] \quad (\text{eq. 1})$$

Recommended minimum $R1 = 1 \text{ M}\Omega$

FPF2281

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V _{IN}	V _{_IN} to GND & V _{_IN} to V _{_OUT} = GND or Float	-0.3	29.0	V
V _{OUT}	V _{_OUT} to GND	-0.3	V _{IN} + 0.3	V
V _{OVLO}	OVLO to GND	-0.3	25.0	V
V _{#EN_ACOK}	Maximum DC Voltage Allowed on #EN or ACOK Pin		6	V
I _{IN}	Switch I/O Current (Continuous)		4.5	A
	Peak Switch I/O Current (10 ms)		9	A
t _{PD}	Total Power Dissipation at T _A = 25°C		1.48	W
T _{STG}	Storage Temperature Range	-65	150	°C
T _J	Maximum Junction Temperature		150	°C
T _L	Lead Temperature (Soldering, 10 Seconds)		260	°C
Θ _{JA}	Thermal Resistance, Junction-to-Ambient ⁽¹⁾ (1-in. ² Pad of 2-oz. Copper)		84.1	°C/W
ESD	IEC 61000-4-2 System ESD	Air Gap	15.0	kV
		Contact	8.0	
	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	3.5	
	Charged Device Model, JESD22-C101	All Pins	2.0	
Surge	IEC 61000-4-5, Surge Protection	V _{IN}	100	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured using 2S2P JEDEC std. PCB

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V _{IN}	Supply Voltage	2.5	25.0	V
T _A	Operating Temperature	-40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

FPF2281

ELECTRICAL CHARACTERISTICS

($T_A = -40^{\circ}\text{C}$ to 85°C unless otherwise indicated. Typical values are $V_{IN} = 5.0\text{ V}$, $I_{IN} \leq 3\text{ A}$, $C_{IN} = 0.1\text{ }\mu\text{F}$ and $T_A = 25^{\circ}\text{C}$.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN_CLAMP}	Input Clamping Voltage	$I_{IN} = 10\text{ mA}$		35		V
I_Q	Input Quiescent Current	$V_{IN} = 5\text{ V}$, $\#EN = 0\text{ V}$		58	100	μA
I_{IN_Q}	OVLO Supply Current	$V_{OVLO} = 3\text{ V}$, $V_{IN} = 5\text{ V}$, $V_{OUT} = 0\text{ V}$		52	100	μA
V_{IN_OVLO}	Internal Over-Voltage Trip Level	V_{IN} Rising	13.6	14.0	14.4	V
		V_{IN} Falling	13.0			V
V_{OVLO_TH}	OVLO Set Threshold	$V_{IN} = 2.5\text{ V}$ to V_{OVLO}	1.12	1.20	1.24	V
V_{OVLO_RNG}	Adjustable OVLO Threshold Range	$V_{IN} = 2.5\text{ V}$ to V_{OVLO}	4		25	V
V_{OVLO_SELECT}	External OVLO Select Threshold			0.30	0.28	V
V_{UVLO}	Under-Voltage Trip Level	V_{IN} Rising, $T_A = -40^{\circ}\text{C}$ to 85°C		2.25	2.4	V
		V_{IN} Falling, $T_A = -40^{\circ}\text{C}$ to 85°C		1.95	2.1	V
R_{ON}	Resistance from V_{IN} to V_{OUT}	$V_{IN} = 5\text{ V}$, $I_{OUT} = 1\text{ A}$, $T_A = 25^{\circ}\text{C}$		30	39	$\text{m}\Omega$
C_{OUT}	OUT Load Capacitance ⁽²⁾	$V_{IN} = 5\text{ V}$			1000	μF
I_{OLVO}	OVLO Input Leakage Current	$V_{OVLO} = V_{OVLO_TH}$	-100		100	nA
T_{SDN}	Thermal Shutdown ⁽²⁾			130		$^{\circ}\text{C}$
T_{SDN_HYS}	Thermal Shutdown Hysteresis ⁽²⁾			20		$^{\circ}\text{C}$

Digital Signals

V_{OL}	#ACOK Output Low Voltage	$V_{IO} = 3.3\text{ V}$, $I_{SINK} = 1\text{ mA}$			0.4	V
$V_{IH_}\#EN$	Enable HIGH Voltage	$V_{IN} = 2.5\text{ V}$ to V_{OVLO}	1.2			V
$V_{IL_}\#EN$	Enable LOW Voltage	$V_{IN} = 2.5\text{ V}$ to V_{OVLO}			0.5	V
I_{ACOK_LEAK}	#ACOK Leakage Current	$V_{ACOK} = 3\text{ V}$, #ACOK Deasserted	-0.5		0.5	μA
$\#EN_Leak$	#EN Leakage Current	$V_{IN} = 5.0\text{ V}$, $V_{OUT} = \text{Float}$	-1.0		1.0	μA

Timing Characteristics

t_{DEB}	Debounce Time	Time from $2.5\text{ V} < V_{IN} < V_{IN_OVLO}$ to $V_{OUT} = 0.1 \times V_{IN}$		15		ms
t_{START}	Soft-Start Time	Time from $V_{IN} = V_{IN_min}$ to $0.2 \times \#ACOK$, $V_{IO} = 1.8\text{ V}$ with $10\text{ k}\Omega$ Pull-up Resistor		30		ms
t_{ON}	Switch Turn-On Time	$R_L = 100\text{ }\Omega$, $C_L = 22\text{ }\mu\text{F}$, V_{OUT} from $0.1 \times V_{IN}$ to $0.9 \times V_{IN}$		2		ms
t_{OFF}	Switch Turn-Off Time ⁽²⁾	$R_L = 100\text{ }\Omega$, $C_L = 0\text{ }\mu\text{F}$, $V_{IN} > V_{OVLO}$ to $V_{OUT} = 0.8 \times V_{IN}$		125		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Guaranteed by characterization and design.

Timing Diagrams

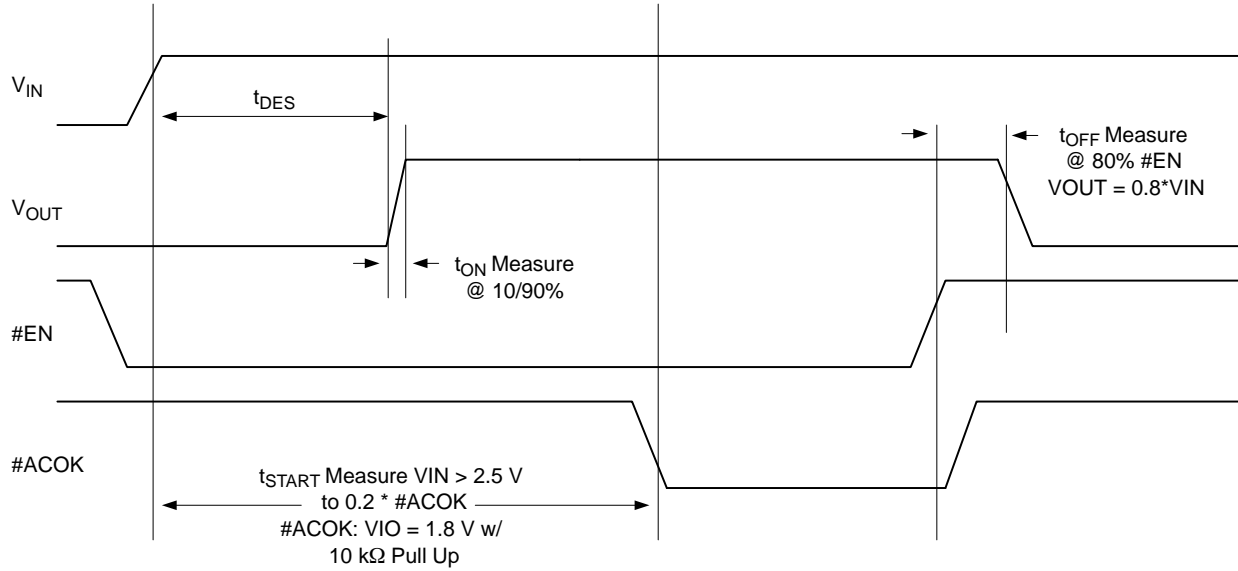


Figure 3. Timing for Power Up and Normal Operation

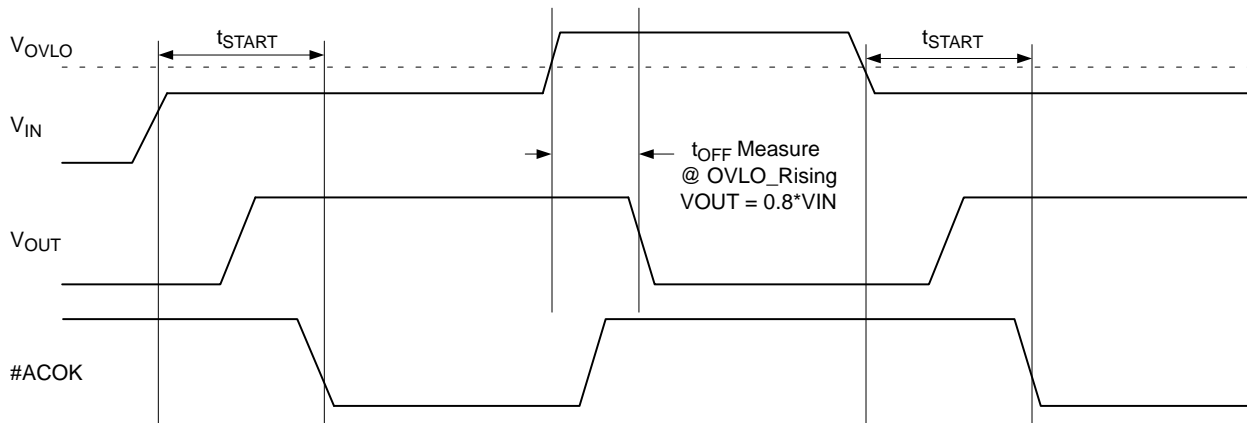


Figure 4. Timing for OVLO Trip

PRODUCT-SPECIFIC DIMENSIONS

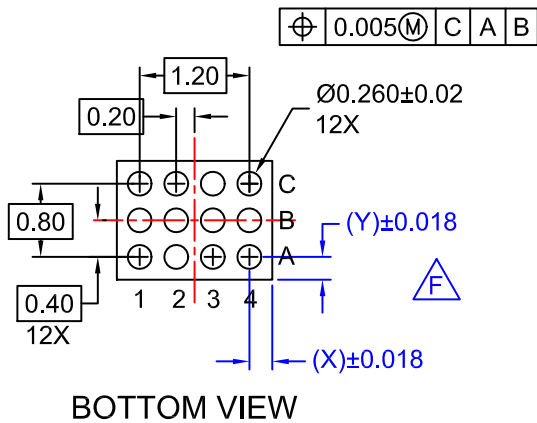
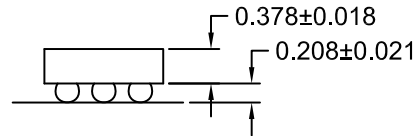
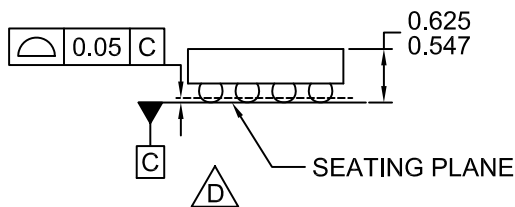
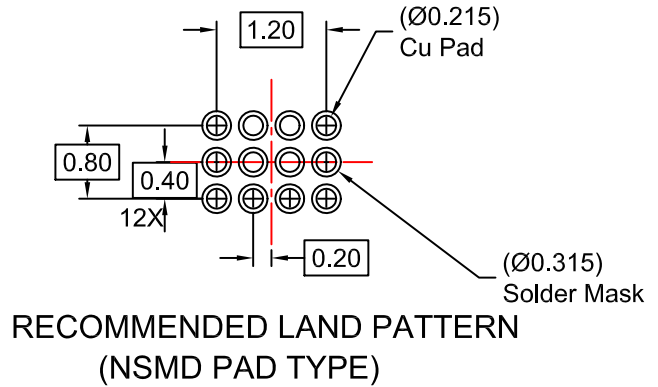
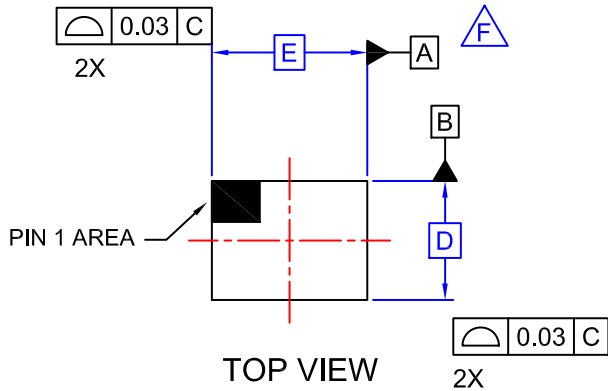
(The table below provides information regarding the WLCSP package on the following page.)

D	E	X	Y
1288 $\mu m \pm 30 \mu m$	1828 $\mu m \pm 30 \mu m$	314 $\mu m \pm 18 \mu m$	244 $\mu m \pm 18 \mu m$



WLCSP12 1.288x1.828x0.586
CASE 567QX
ISSUE O

DATE 31 OCT 2016



NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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